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S5200E DS3

DIGITAL TRANSMISSION TEST SET

TRANSMITTER
OPERATION MANUAL

FORM 0337-0585A

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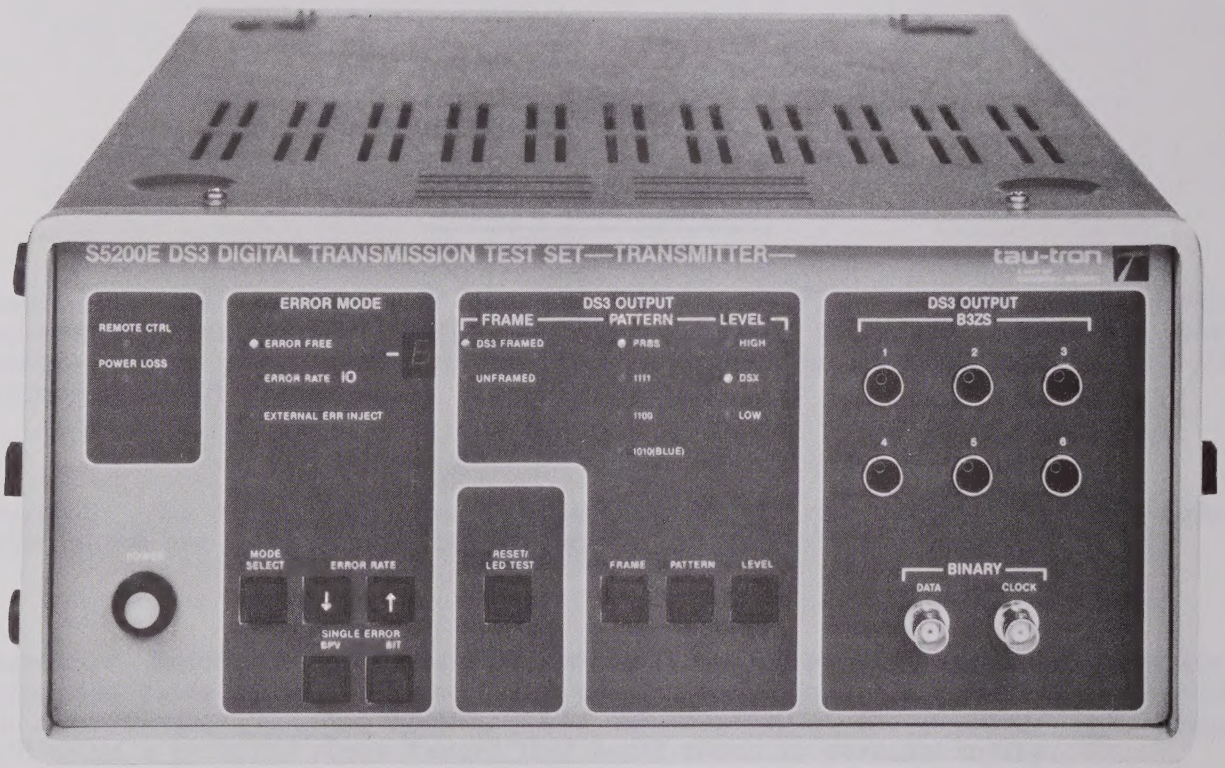

S5200E DS3

DIGITAL TRANSMISSION TEST SET

TRANSMITTER
OPERATION MANUAL

FORM 0337-0585A

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(617) 692-5100 Telex 750245 1-800-TAU-TRON (Outside MA)

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SAFETY INFORMATION

Caution: This instrument is designed to operate from a single phase power source, with one of the current carrying conductors at ground. Operation from power sources where both current carrying conductors are live with respect to ground is not recommended.

Warning: To avoid dangerous electrical shock, do not perform electrical tasks when there are signs of shipping damage to any part of the instrument case.

Warning: Before the instrument is switched on, all protective ground terminals, extension cords, autotransformers and devices connected to it should be connected to a protective grounded socket. Any interruption of the protective grounding will cause a potential shock hazard that could result in personal injury.

WARRANTY

All Tau-tron products are warranted against any defects in material and workmanship. This warranty applies for one year from the date of delivery for all Tau-tron manufactured products. The warranty period for OEM products sold by Tau-tron will depend on the original OEM warranty (consult factory for specific products). We will repair or replace products which, upon our examination, prove to be defective during the warranty period.

NO OTHER WARRANTY, EXPRESS OR IMPLIED, INCLUDING FITNESS FOR PURPOSE, MERCHANTABILITY OR OTHERWISE, IS GIVEN.

For assistance, contact Customer Service with details of the instrument model, serial numbers, and malfunction; see Repair Returns below.

SHIPPING DAMAGE

If any signs of damage are noted on the outside of the carton, request that the carrier's agent be present during unpacking. If external damage is found on the instrument, follow Repair Returns procedure below.

Check the electrical performance of the instrument as soon as possible after receipt. If any malfunctions are observed, follow Repair Returns procedure below.

REPAIR RETURNS

For mechanical damage or electrical malfunctions, notify Tau-tron immediately. If the damage occurred during shipping, also notify the carrier. To return a unit for repair:

1. Call the Customer Service Department, (617) 692-5100, for a Repair Authorization Number. This will reduce administrative delays and ensure prompt return of your unit.

2. Complete and attach the Repair Tag, in the rear of the manual, to your unit for positive identification.

3. Pack the unit in the original shipping carton and packing materials, if available. Otherwise use a double-walled carton (test strength of 350 lb; 159 kg) and shock-absorbing material such as bubblewrap to prevent the unit from moving in the carton during transit. Secure the carton by sealing with heavy paper tape.

4. Send to: Tau-tron Inc.
   10 Lyberty Way
   Westford, MA 01886
   Attn: Customer Service

S5200E DS3

DIGITAL TRANSMISSION TEST SET TRANSMITTER

CONTENTS PAGE

1. INTRODUCTION 1/2
A. General 1/2
B. Scope 1/2
C. Errors, Omissions, and Recommendations.....1/2
2. DESCRIPTION 3
A. General 3
3. SPECIFICATIONS 5
A. General 5
4. OPERATION 9
A. General 9
B. Power Connection and Power-up Procedure 9
C. Front Panel Controls, Indicators, and Connectors ...10
D. Rear Panel Controls and Connectors.....16
5. THEORY OF OPERATION 21
A. General 21
B. Plug-in Boards and Front-Panel Board Theory of Operation 21
C. Software Theory of Operation 29
D. Power Distribution 30
6. SERVICE AND MAINTENANCE 33
A. Assistance 33

CONTENTS PAGE

B. Repair Returns.....33
C. Routine Service 33
D. General Troubleshooting 33
E. Software Diagnostics 34
APPENDIX A
DS3 TESTING 35
A. General 35
B. DS3 Signal Format.....35
C. Parity Error Testing 36
D. Frame Error Testing.....37
E. Bit Error Testing 38
F. Bipolar-Pulse-Violation (BPV) Testing 38
G. System Characterization Using Error Seconds.....40
APPENDIX B
IEEE-488 INTERFACE (GPIB) 43
A. General 43
B. Introduction 43
C. GPIB Interface Connections...44
D. S5200E Response to GPIB Commands 45
E. Device Dependent Commands..48
F. Service Request and Serial Poll Response 51
G. Sample GPIB Control 53

CONTENTS PAGE

APPENDIX C
PERFORMANCE VERIFICATION.....57

A. General 57

B. Transmitter Performance Verification Tests 57

C. Transmitter Performance Verification with Receiver Tests 60

APPENDIX D
RACK MOUNT OPTION
INSTALLATION 65

FIGURES PAGE

1. S5200E Transmitter Front and Rear View 4

2. AC Power Connector and Fuse Housing 10

3. Front Panel Controls, Indicators, and Connectors 10

4. Rear Panel Controls and Connectors 17

5. S5200E Transmitter Internal Board Assembly 22

6. Transmitter System Functional Block Diagram 23/24

7. Oscillator Interface Board Functional Block Diagram 25

8. Transmit Generator Board Functional Block Diagram 25

9. Output Amplifier Board Functional Block Diagram 26

10. STD Interface Board Functional Block Diagram 27

FIGURES PAGE

11. GPIB Board Functional Block Diagram 28

12. CPU Board Functional Block Diagram 28

13. Front Panel Display Board Functional Block Diagram 29

14. S5200E Transmitter Power Distribution 31/32

15. Power Supply Voltage Test Points and Nickel Cadmium Battery Location 34

16. DS3 Signal Format 35

17. System Testing for Parity Errors 37

18. System Testing for Bit Errors 39

19. Synchronous and Asynchronous Error-Second Format 40

20. GPIB Address DIP Switch Setting 44

21. Rackmount Installation 65

TABLES PAGE

A. S5200E Transmitter Specifications ..5

B. Front Panel Controls, Indicators and Connectors 11

C. Rear Panel Controls and Connectors 17

D. Error Thresholds 42

E. GPIB DIP Switch Settings 45

F. Device-Dependent Commands.....50

SECTION 1

INTRODUCTION

1. INTRODUCTION

A. General

1.01 This manual provides the user with all information required for the installation, operation, and maintenance of the Tau-tron S5200E Digital Transmission Test Set Transmitter.

1.02 Whenever this manual is reissued, the reason for the reissue will be given in this paragraph.

B. Scope

1.03 The following information is provided:

- Equipment description
- Specifications
- Installation instructions and site requirements
- Operation instructions
- Theory of operation
- Maintenance.

C. Errors, Omissions, and Recommendations

1.04 We would appreciate your comments about any errors or omissions you discover in this manual. When reporting errors or omissions, please be specific and indicate the section number, title, and page number. Also, indicate the paragraph number, figure number, or table designation.

1.05 Your recommendations for improving the quality, contents, and usability of this document are requested and solicited. Please address all correspondence to:

Tau-tron Inc.
ATTN: PUBLICATIONS MANAGER
10 Lyberty Way
Westford, MA 01886

SECTION 2

DESCRIPTION

2. DESCRIPTION

A. General

2.01 The Tau-tron S5200E Digital Transmission Test Transmitter, together with the S5200E Digital Transmission Test Receiver, form a compact test set for detailed measurements of systems operating at the DS3 transmission rate.

2.02 The S5200E Transmitter can generate the standard DS3-compatible 2^{15}-1 pseudorandom sequence with or without DS3 framing. The absence of framing allows measurements of switching-time faults in radio systems and the number of errors generated during a switch, and allows testing of satellite systems using unframed signals at the DS3 rate. Use of a pseudorandom sync pulse on both the transmitter and the receiver permits measurements of variations in transit time in satellite patterns.

2.03 The DS3 signal generated by the S5200E Transmitter is a bipolar signal with B3ZS coding and can be set to one of three levels: HIGH, DSX, or LOW. This signal is output through 6 front panel jacks simultaneously.

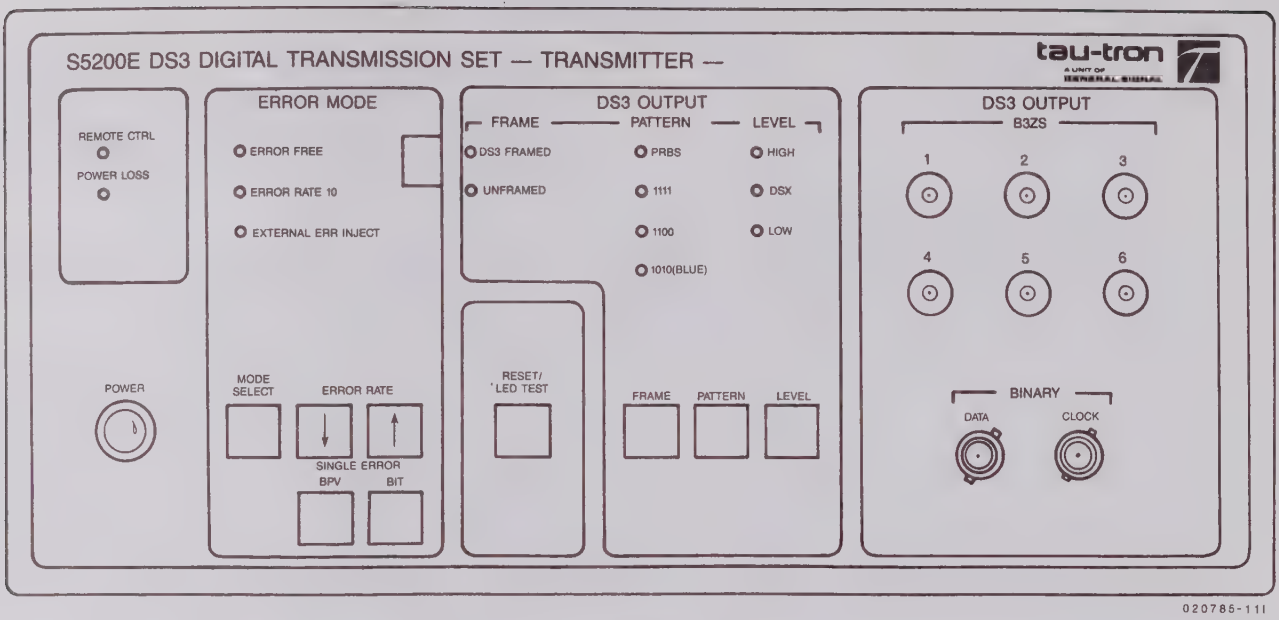
2.04 There are four data patterns that can be selected by the operator: PRBS, the standard 2^{15}-1 pseudorandom sequence, and three short patterns, 1111, 1100, and 1010. The 1010 pattern in the framed mode is referred to as the Blue pattern.

2.05 Binary, NRZ coded, Data and Clock signals are output through front panel BNC connectors.

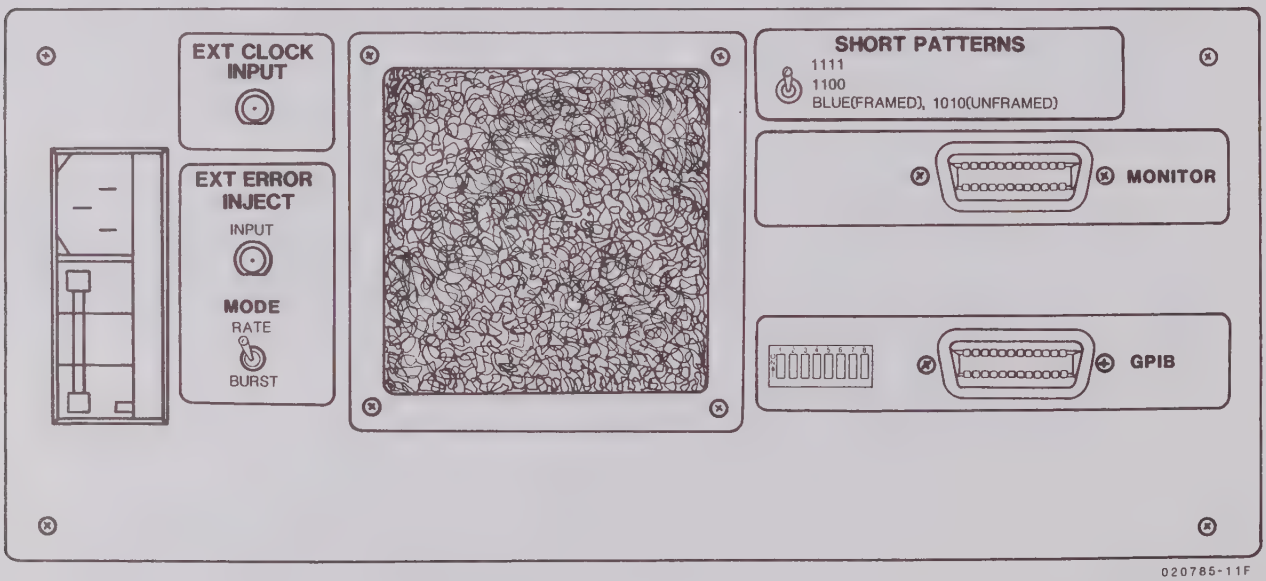
2.06 Internally generated transmission errors are developed in a manner that assures an even statistical distribution of errors over all output bits. Error injection rates of $1x10^{-N}$, where $N = 1,2, \ldots 9$, can be selected by the operator. Error rates other than the fixed internal rates can be generated by using the external error-rate or error-burst modes.

2.07 If the S5200E Transmitter contains the optional IEEE-488 (GPIB) interface, the operator has the ability to operate all the functions of the transmitter through remote control.

2.08 The front and rear panels of the S5200E Transmitter are illustrated in Fig. 1. A review of the following section will acquaint the operator with the complete specifications of the transmitter.



FRONT PANEL



REAR PANEL

Fig. 1 - S5200E Transmitter Front and Rear View

SECTION 3

SPECIFICATIONS

3. SPECIFICATIONS

A. General

3.01 This section describes all the specifications of the S5200E Digital Transmission Test Transmitter.

TABLE A

S5200E TRANSMITTER SPECIFICATIONS

ITEM	DESCRIPTION
INTERNAL CLOCK	
Frequency	44.736 MHz ±20 ppm at 0° to 50°C (32°F to 122°F).
EXTERNAL CLOCK	
Frequency	44.736 MHz ±3 MHz.
Level	AC coupled, 800 MV peak-to-peak minimum. Sine wave, maximum level 5 volts.
Impedance	75-ohm load.
Connector	BNC, rear panel.
DATA PATTERNS	
PRBS	Repeating pseudorandom bit sequence of $2^{15}-1 = 32,767$ bits.
Short Patterns	All ones. Repeating 1100. Repeating 1010.
Blue Signal	DS3 Framed 1010 repeating sequence; logical one data bit follows frame bit.
FRAMING	
Framed	Bell-compatible DS3 framing format.
Unframed	No framing bits, data pattern output only, at the clock frequency.

TABLE A (CON'T)

S5200E TRANSMITTER SPECIFICATIONS

ITEM	DESCRIPTION
BIPOLAR OUTPUTS	
Coding	Bipolar with 3 zero substitution.
Level:	
HIGH Output	0.91V peak nominal.
LOW Output	13.8dB below nominal High, 0.186V peak nominal.
DSX Output	High output passed through equivalent of 450 feet (114.3 m) of 728A cables, typically 5 to 6 dB below HIGH, 0.48V peak typical.
Impedance	75-ohm source.
Connector	Accepts WECo 358.
Quantity	Six identical outputs.
BINARY DATA & CLOCK OUTPUTS	
Coding	Non-return to zero (NRZ).
Level	Logic 1 = +1V, Logic 0 = -1V (into 75 ohm load).
Phasing	Rising clock edge in center of data ±4 ns.
Impedance	75-ohm source.
Connector	BNC.
ERROR INJECTION	
Internal Error:	
General	Error-rate injection on output signal. In the unframed mode, errors are on data bits. In framed mode, errors are in data and DS3 framing bits affecting bit and parity.

TABLE A (CON'T)

S5200E TRANSMITTER SPECIFICATIONS

ITEM	DESCRIPTION
ERROR INJECTION (con't)	
Method	A non-periodic insertion to insure even statistical error distribution over all bits.
Rate	1×10^{-N} for N = 2 thru 9 in increments of 1.
Single Errors	Single bit or single bipolar violation (BPV).
External Error:	
General	External bit errors inserted by applying external generator. In rate mode, errors are proportional to frequency. In burst mode, errors occur during positive cycle of external input.
Level	TTL level.
Impedance	300-ohm source.
Rate	Any error-rate less than approximately 450K errors/sec.
Burst	100% errors during positive portion of waveform. 10-bit error burst minimum.
MONITOR	
Outputs	Pseudorandom data pattern sync, M-Sync, PR-Sync. Power Fail latching indication of previous lost input power. M-Sync is a pulse with a 106 µs period. PR-Sync is a pulse with a 741 µs period.
Input	X-Bit, TTL low or ground to change X-Bit from normal logic 1 to 0.
Level	TTL compatible.
Interface	24-pin D-connector on rear panel.
POWER	115 VAC, 50 to 60 Hz, 60 VA maximum. AC input can be either sine wave or square wave.

TABLE A (CON'T)

S5200E TRANSMITTER SPECIFICATIONS

ITEM	DESCRIPTION
MECHANICAL:	
Height	6.6 in. (23.4 cm).
Width	13.6 in. (34.5 cm).
Depth	19.8 in. (50.3 cm).
Weight	19 lb. (8.6 kg).
ENVIRONMENTAL:	
Temperature	32° to 104°F (0° to 40°C).
Humidity	0 to 95% relative humidity at 20°C (68°F), non-condensing.
OPTIONS:	
IEEE-488 (GPIB) Interface	For remote control.
Rack Mount Kit	Adapts instrument for mounting in a standard 19-in. (48.3cm) rack.
5910 Power Converter	Converts -24 to -48VDC input to 115VAC output.
5902 Printer	40-column printer.
Hard-Shell Shipping Case	Foam-lined fiberglass case.
Soft Carrying Case	Foam-lined canvas carrying case.

SECTION 4

OPERATION

4. OPERATION

A. General

4.01 This section describes the use of all controls, connectors, and indicators of the S5200E Digital Transmission Test Set Transmitter. The performance verification procedure in Appendix C can be used to check that the Transmitter is functioning properly. It is also an excellent introduction to the operation and capabilities of the S5200E Transmitter.

4.02 The S5200E Transmitter front and rear panels are divided into sections of functionally related controls, indicators, and connectors. These sections are keyed by number in the front and rear panel illustrations of this section (see Figs. 3 and 4). Use the number keys to locate information about a control, indicator, or connector in the table following the illustration (Table B or Table C).

B. Power Connection and Power-Up Procedure

4.03 The correct procedure for making power connections and powering ON the S5200E Transmitter is as follows:

STEP	PROCEDURE
1	Check that the POWER Switch/Indicator is in the OFF position (In = ON, Out = OFF).
2	At the fuse housing on the rear panel, slide the plastic cover to the left to expose the fuse (see Fig. 2).
3	Push the FUSE PULL lever to the left, remove the fuse, and check to see that it is rated 2A slow-blow.
4	Check that the legend on the PC card in the fuse housing reads 120V. The 120V legend must be face-up and inserted as shown in Fig. 2. If this is not the case, remove the PC card (pull straight out), turn it around, and reinsert. The PC card is also marked for 240V, 100V, and 220V, but these ranges are not available for this unit.
5	Push the FUSE PULL lever to the right, back to its normal position, and reinstall the fuse.
6	Connect the 3-wire, AC power cord to the 3-prong connector of the S5200E Transmitter. Green = Ground, Black = Hot, White = Neutral.
7	Connect the male end of the AC power cord to a 115 VAC power source.
8	Push the POWER Switch/Indicator in, to the ON position. The Indicator should light showing that the unit is on.

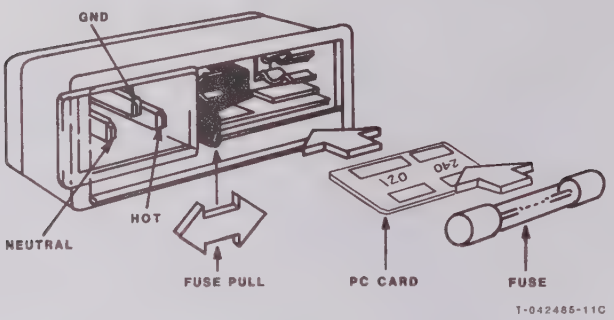


Fig. 2 - AC Power Connector and Fuse Housing

C. Front Panel Controls, Indicators, and Connectors

4.04 The S5200E Transmitter front panel contains most of the controls and all of the indicators used to select or set the parameters of the signals output by the S5200E Transmitter. Also contained on the front panel are the DS3 bipolar and binary output connectors.

4.05 Table B explains the function of all the front panel controls, indicators, and connectors of the S5200E Transmitter.

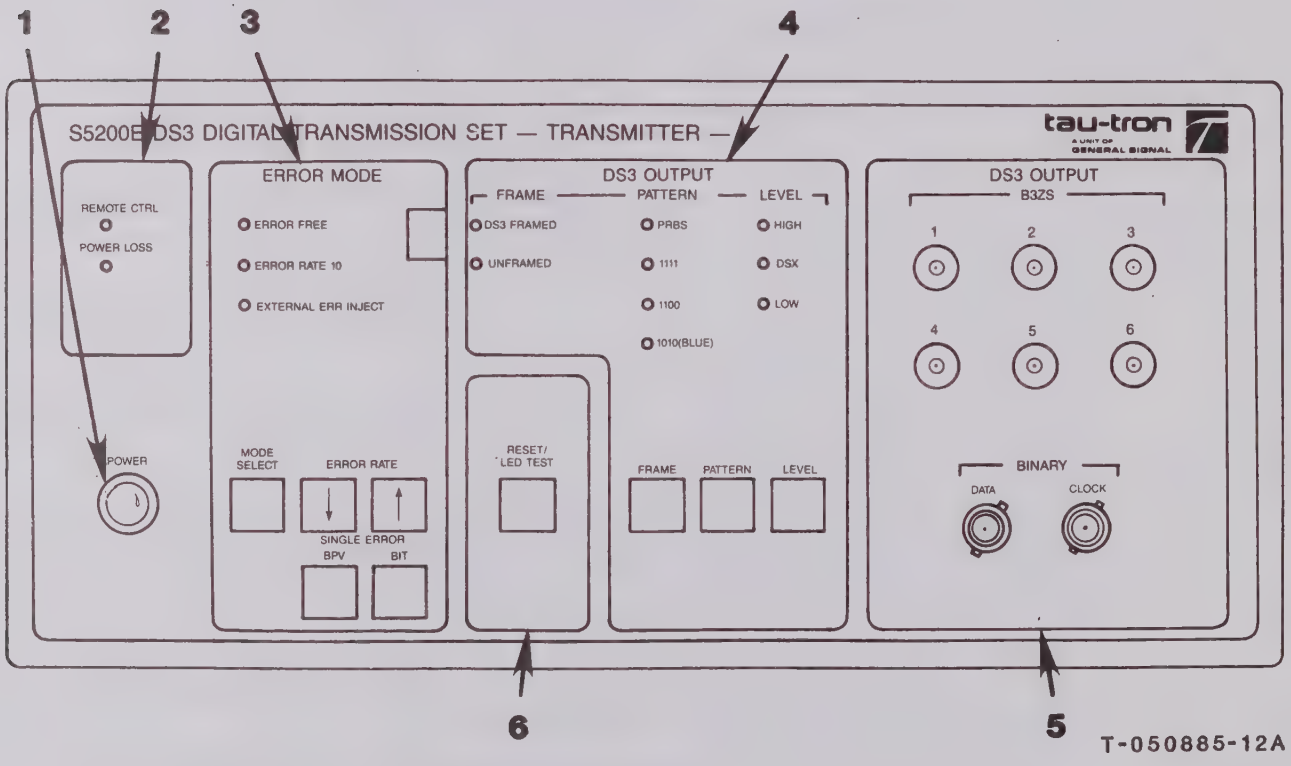


Fig. 3 - Front Panel Controls, Indicators, and Connectors

TABLE B

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
1	POWER (Switch/Indicator)	When pressed in, power is ON, and the indicator lights. The Transmitter does not have a specific power-on state. It will power up in the same state it was in when it was last turned off. If the IEEE-488 Interface is installed, some initial self-diagnostics are run before initialization is complete. Three 1.2 Vdc Nickel Cadmium batteries, inside the S5200E Transmitter, provide the Transmitter with a power-fail recovery capability. If the Transmitter was under GPIB remote control, during the power failure, it would return to local control.
2	REMOTE CTRL (indicator)	Lights when the Transmitter is under remote control. This occurs when the Transmitter is addressed to listen and the REN (remote enable) line of the GPIB is asserted. If the Transmitter is not configured with the IEEE-488 Interface option, then this indicator will not be functional.
	POWER LOSS (indicator)	Lights when the Transmitter is initially turned ON and/or if there is a disruption of power. Pressing the RESET/LED TEST pushbutton causes the indicator to extinguish.
3	ERROR MODE	This section contains the pushbuttons and indicators which are used to select the error mode and error rate or to inject single BPV or bit errors.
	MODE SELECT (pushbutton)	Selects one of three available error modes: ERROR FREE, ERROR RATE 10^{-N}, or EXTERNAL ERR INJECT. Each time the pushbutton is pressed, it switches to the next mode, lighting the appropriate indicator.

TABLE B (CON'T)

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
3	ERROR FREE (indicator)	Lights when the ERROR FREE mode is selected. In this mode of operation the output data is transmitted without errors.
	ERROR RATE 10^{-N} (indicator)	Lights when the internal bit ERROR RATE injection mode is selected. N is the exponent of the bit error rate and is an integer from 2 to 9 displayed in the single digit LED display. Therefore, eight error rates from 10^{-2} to 10^{-9} can be inserted into the output data pattern in the DS3 FRAMED or UNFRAMED mode of operation. In the DS3 FRAMED mode, errors are inserted in both the information bits and the DS3 frame bits. The ERROR RATE is selected by the ERROR RATE pushbuttons. The single digit display brightens when the ERROR RATE 10^{-N} mode is selected.
	EXTERNAL ERR INJECT (indicator)	Lights when the EXTERNAL ERR INJECT mode is selected. BURST errors and RATE errors can be externally generated and inserted into the output data format by using an external oscillator connected to the rear-panel EXT ERROR INJECT INPUT BNC connector. In the BURST MODE, the error burst rate is 100% errors during the time the oscillator input is high. In the RATE MODE, an error is introduced at each positive going transition at rates up to 450,000 errors per second.
	ERROR RATE ↓ and ↑ (pushbuttons)	These pushbuttons are used to select the internal bit ERROR RATE. The ↓ (down arrow) ERROR RATE pushbutton decreases the ERROR RATE value (larger number appears in the single digit display when pressed) and the ↑ (up arrow) ERROR RATE pushbutton increases the ERROR RATE value (smaller number appears in the single digit display when pressed).

TABLE B (CON'T)

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
3	SINGLE ERROR BPV (pushbutton)	Inserts a single Bipolar Pulse Violation (BPV) into the output data pattern when pressed. This is true when the Transmitter is in either the DS3 FRAMED or the UNFRAMED mode of operation. Single errors can be inserted in any ERROR MODE. However, unless the selected ERROR MODE is ERROR FREE, pressing the SINGLE ERROR BPV pushbutton may override an error being inserted, resulting in no error.
	SINGLE ERROR BIT (pushbutton)	Inserts a single bit error into the output data pattern when pressed. This is true whether the Transmitter is in the DS3 FRAMED or in the UNFRAMED mode of operation. Single errors can be inserted in any ERROR MODE. However, unless the selected ERROR MODE is ERROR FREE, pressing the SINGLE ERROR BIT pushbutton may override an error being inserted, resulting in no error.
4	DS3 OUTPUT FRAME-PATTERN-LEVEL	This section contains the pushbuttons and indicators to set the format of the DS3 output signal.
	FRAME (pushbutton)	Selects the frame mode of the Transmitter output signal, either DS3 FRAMED or UNFRAMED. Pressing the FRAME pushbutton switches between the DS3 FRAMED and UNFRAMED modes, lighting the appropriate indicator.
	DS3 FRAMED (indicator)	Lights when the DS3 FRAMED mode is selected. In this mode, the data pattern is interspersed with the DS3 housekeeping bits. One in every 85 output bits will be a DS3 housekeeping or Framing bit which include X-bits, Parity bits, M-bits, F-bits, and C-bits. For more detailed information on DS3 framing and frame bits, see Appendix A.

TABLE B (CON'T)

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
4	UNFRAMED (indicator)	Lights when the UNFRAMED mode is selected. In this mode, no DS3 frame bits are inserted into the DS3 output signal.
	PATTERN (pushbutton)	Selects the data pattern of the DS3 and Binary output signals. Pressing the PATTERN pushbutton switches the selection between PRBS (pseudorandom bit sequence) and a short pattern: 1111, 1100, or 1010 (BLUE). The short pattern is selected by the rear-panel SHORT PATTERNS toggle switch (See Table C, #5). In the framed mode, there is no synchronization between the PRBS or short pattern data bits and the framing bits. The PRBS or pseudorandom bit sequence is the Bell standard 2^{15}-1 bit sequence. The short pattern sequences: 1111, 1100, and 1010 are set by the rear-panel SHORT PATTERNS toggle switch. These data patterns appear at the Transmitter outputs in the UNFRAMED mode or are interspersed with DS3 framing bits in the DS3 FRAMED mode. If the Transmitter is in the DS3 FRAMED mode, the 1010 data sequence becomes the BLUE signal, which is often used in multi-hop radio systems. In this application a failed hop will generate the BLUE signal and transmit it down the system to inhibit downstream alarms in the DS3 transmission system. The BLUE signal should also cause all connected channel banks to go into Carrier Group Alarm.
	1111 (indicator)	Lights when the 1111 PATTERN is selected. See PATTERN pushbutton.
	1100 (indicator)	Lights when the 1100 PATTERN is selected. See PATTERN pushbutton.
	1010 (BLUE) (indicator)	Lights when the 1010 (BLUE) PATTERN is selected. See PATTERN pushbutton.

TABLE B (CON'T)

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
4	LEVEL (pushbutton)	Selects the desired DS3 output LEVEL: HIGH, DSX, or LOW. Pressing the LEVEL pushbutton switches the Transmitter to the next output LEVEL, lighting the appropriate indicator. Binary outputs are not affected by the LEVEL pushbutton.
	HIGH (indicator)	Lights when the HIGH DS3 output level is selected. Nominal HIGH output is 0.91V peak.
	DSX (indicator)	Lights when the DSX DS3 output level is selected. The DSX output signal is a HIGH output passed through the equivalent of 450 feet (114.3 m) of 728A cable. It is typically 5 to 6 dB below the HIGH output level, 0.48V peak typical.
	LOW (indicator)	Lights when the LOW DS3 output level is selected. The LOW output is 13.8dB below the nominal HIGH output level, 0.186V peak nominal.
5	DS3 OUTPUT	This section contains the connectors which output the B3ZS (bipolar) and BINARY DS3 signals.
	B3ZS (connectors)	Six identical connectors which accept WECo 358 plugs. The connectors may be used simultaneously. They output the DS3 bipolar B3ZS signal generated by the Transmitter at any of three levels selected from #4 above. Connections should be through a 75-ohm cable to a 75-ohm load.
	BINARY DATA and CLOCK (connectors)	BNC connectors which have a 75-ohm source impedance. Levels are ±1V peak centered around 0V into a 75-ohm load. Data format is non-return to zero (NRZ). The positive clock edge is in the center of the data bit. This data clock phasing can be changed 180° by using unequal data and clock cables with an 8-foot (2.4 m) differential. When using the BINARY outputs, be sure the equipment

TABLE B (CON'T)

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
5	BINARY DATA and CLOCK (connectors) (con't)	being tested is compatible with the level and phasing characteristics of the S5200E Transmitter. NOTE: Cables should be of equal length for positive clock edge in the center of the data bit, and equipment under test should have a 75-ohm input impedance.
6	RESET/LED TEST (pushbutton)	When the RESET/LED TEST pushbutton is pressed in and held, all front-panel indicators will light. This is a good test to prove all indicators are functioning. When the pushbutton is released, the POWER LOSS indicator will extinguish.

D. Rear Panel Controls and Connectors

4.06 The S5200E Transmitter rear panel contains connectors for external error injection and clock input, the short pattern selection toggle switch, a monitor connector, and a GPIB interface connector and DIP switch.

4.07 Table C explains the function of all the rear panel switches and connectors of the S5200E Transmitter.

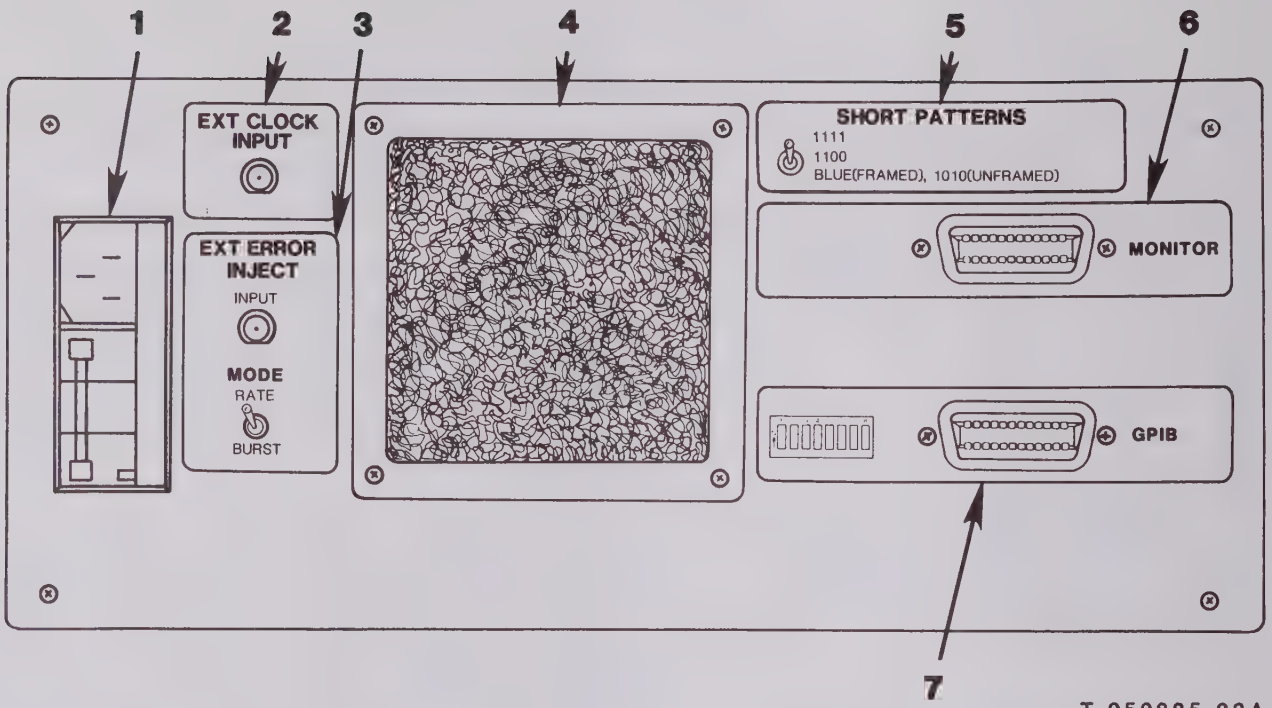


Fig. 4 - Rear Panel Controls and Connectors

TABLE C

REAR PANEL CONTROLS AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
1	AC Power Connector/ Fuse Housing	Contains the 3-prong AC power connector and fuse. For complete detail information see section 4B, Power Connection and Power-Up Procedure.
2	EXT CLOCK INPUT (connector)	BNC connector used to accept an external clock signal. The input impedance is 75 ohms, AC coupled and requires an 800 mV minimum peak-to-peak level (sine wave). When this 800 mV level is reached, the Transmitter will automatically switch to the external clock signal and switch off the internally generated clock signal. The maximum level is 5 volts. The input range of the accepted external clock signal is 44.736 MHz ±3 MHz.

TABLE C (CON'T)

REAR PANEL CONTROLS AND CONNECTORS

NO	DESIGNATION	DESCRIPTION
3	EXT ERROR INJECT INPUT (connector)	BNC connector, accepts a signal from an external oscillator which generates errors. The external oscillator must be capable of driving 300 ohms, and its waveform must swing from less than 0.5V to greater than 3V peak. The externally generated BURST or RATE errors are inserted into the output data format.
	MODE RATE/BURST (toggle switch)	Selects either the RATE or the BURST error mode of external error injection signal applied to the EXT ERROR INJECT INPUT connector. In the BURST MODE, the error burst rate is 100% errors during the time the external oscillator input is high. In the RATE MODE, an error is introduced at each positive going transition at rates up to 450,000 errors per second.
4	Fan	Air intake fan for internal cooling and heat dissipation.
5	SHORT PATTERNS 1111/1100/Blue (Framed); 1010 (UNFRAMED) (toggle switch)	Three-position toggle switch used to set the short pattern format for the front-panel OUTPUT PATTERN selection (see PATTERN pushbutton in Table B).
6	MONITOR (connector)	24-pin D-connector with inputs and outputs used for external monitoring. A mating connector is supplied with the S5200E Transmitter. The MONITOR provides the following: Sync Outputs - There are 2 sync outputs, M sync and PR sync. M sync occurs once per DS3 Master Frame (4760 bits). PR sync occurs once per 2^{15}-1 bits of the Pseudo-random Sequence Generator. The following pins output the M sync and PR sync:

TABLE C (CON'T)

REAR PANEL CONTROLS AND CONNECTORS

<table>
<tr><th>NO</th><th>DESIGNATION</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>MONITOR (connector) (con't)</td><td>
<table>
<tr><th>PIN</th><th>FUNCTION</th><th>ACTIVITY</th></tr>
<tr><td>7</td><td>M sync</td><td>Positive pulse, TTL level with 5.1 kohm to +5V.</td></tr>
<tr><td>18</td><td>M sync</td><td>Negative pulse, TTL level with 5.1 kohm to +5V.</td></tr>
<tr><td>17</td><td>PR sync</td><td>Positive pulse, TTL level with 5.1 kohm to +5V.</td></tr>
<tr><td>5</td><td>PR sync</td><td>Negative pulse, TTL level with 5.1 kohm to +5V.</td></tr>
</table>
Power Loss Status - A power loss status is provided on the MONITOR connector. Whenever power is lost due to a power failure or when the S5200E Transmitter is turned ON, the POWER LOSS status will latch until the RESET/LED TEST pushbutton is pressed. The following pins on the MONITOR connector are used to monitor power loss status:
<table>
<tr><th>PIN</th><th>FUNCTION</th><th>ACTIVITY</th></tr>
<tr><td>10</td><td colspan="2">Power Loss Active high, TTL level with 5.1 kohm to +5V.</td></tr>
<tr><td>22</td><td colspan="2">Power Loss Active low, TTL level with 5.1 kohm to +5V.</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>GPIB Interface Connector and DIP Switch</td><td>An IEEE-488 Interface connector and DIP switch used to interface the General Purpose Interface Bus (GPIB) capabilities of the S5200E Transmitter with other GPIB devices. For detailed information of the GPIB Interface operation, see Appendix B.</td></tr>
</table>

SECTION 5

THEORY OF OPERATION

5. THEORY OF OPERATION

A. General

5.01 This section explains the theory of operation and the power distribution of the S5200E Transmitter.

5.02 The S5200E Transmitter consists of four plug-in printed circuit boards, a front-panel display board, and a rear-panel control board. If the IEEE-488 (GPIB) Interface option is installed in the S5200E Transmitter, two additional plug-in printed circuit boards are installed. Two power supplies are used in the Transmitter: a +5V power supply at 12A and a -5.2V power supply at 6A. Figure 5 illustrates the assembly layout of the Transmitter and Figure 6 is a general functional block diagram of the Transmitter system.

5.03 The plug-in boards can be divided into two functional sections: a High-Speed section and a Software/ Hardware section. The plug-in boards are divided as follows:

High-Speed section:

- Oscillator Interface board
- Transmit Generator board
- Output Encoder-Amplifier board

Software/Hardware section:

- STD Interface board
- CPU board (IEEE-488 installed)
- GPIB board (IEEE-488 installed)

5.04 All the plug-in boards plug into a Mother Board which is divided into the High-Speed and Software/ Hardware sections. The Software/ Hardware section uses an STD 8-bit microprocessor system bus.

5.05 If the S5200E Transmitter has the IEEE-488 (GPIB) option installed, 2 plug-in printed circuit boards are added: the CPU board and the GPIB board. In addition, the STD Interface board is built-up to provide a switching capability between local front-panel control and remote GPIB control.

B. Plug-in Boards and Front-Panel Board Theory of Operation

Oscillator Interface Board

5.06 The Oscillator Interface board (see Fig. 7) contains a 44.736 MHz crystal-controlled oscillator that feeds its output through an ECL driver circuit to the Transmit Generator board. In addition, the Oscillator Interface board contains circuitry to detect an external clock signal input applied to the rear-panel EXT CLOCK INPUT BNC connector. This circuitry switches out the internal oscillator and switches in the external clock signal when an external signal is detected.

5.07 A circuit on the Oscillator Interface board converts the ECL data and timing signals, from the Transmit Generator board, to NRZ (non-return to zero). The NRZ signals are output to the front-panel BINARY DATA and CLOCK BNC connectors.

5.08 The M-Sync and PR-Sync signals from the Transmit Generator board are output through the Oscillator Interface board to the rear-panel MONITOR connector. The external error-injection signal from the rear-panel EXT ERROR INJECT INPUT BNC connector is output through the Oscillator Interface board to the Transmit Generator board.

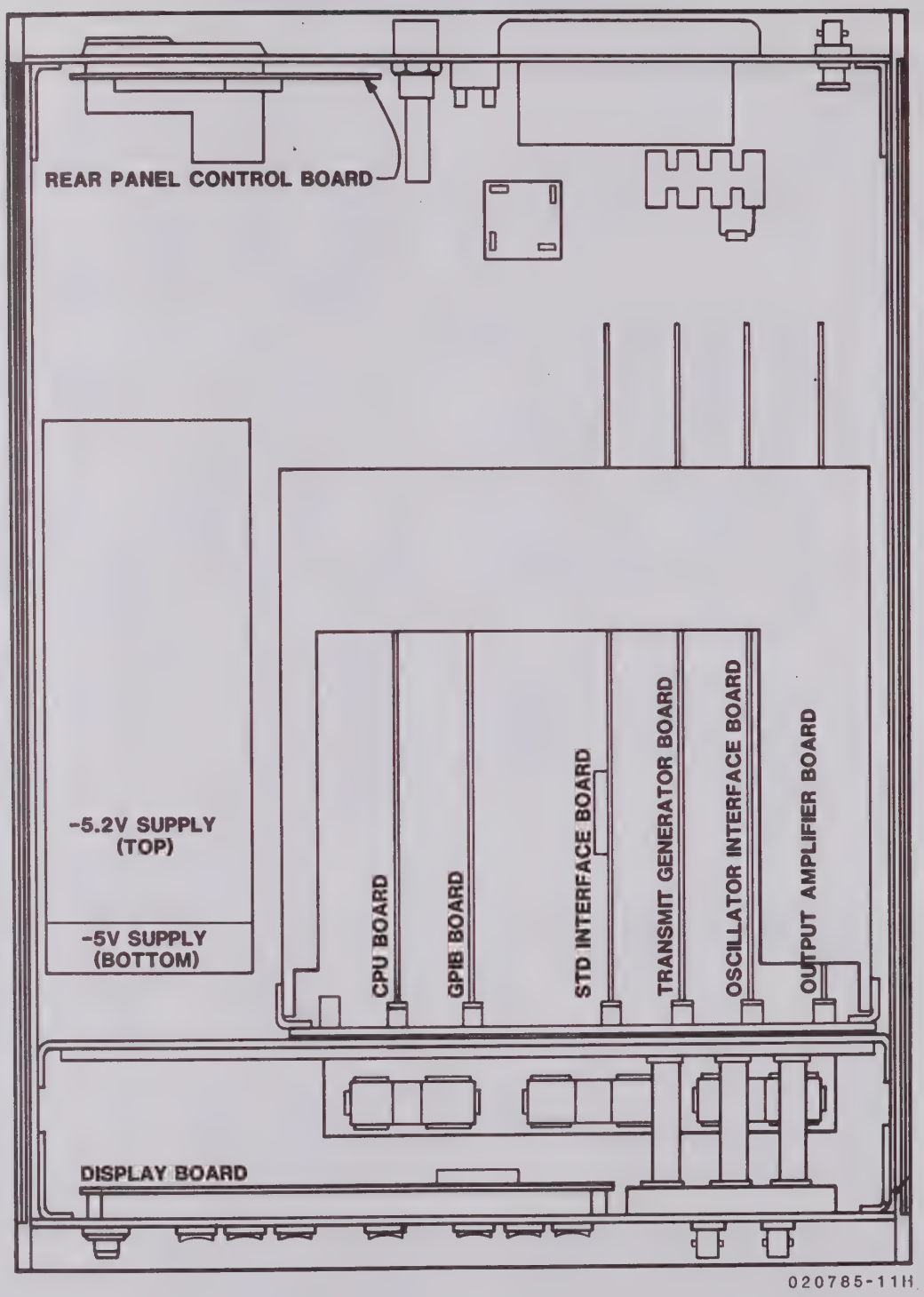


Fig. 5 - S5200E Transmitter Internal Board Assembly

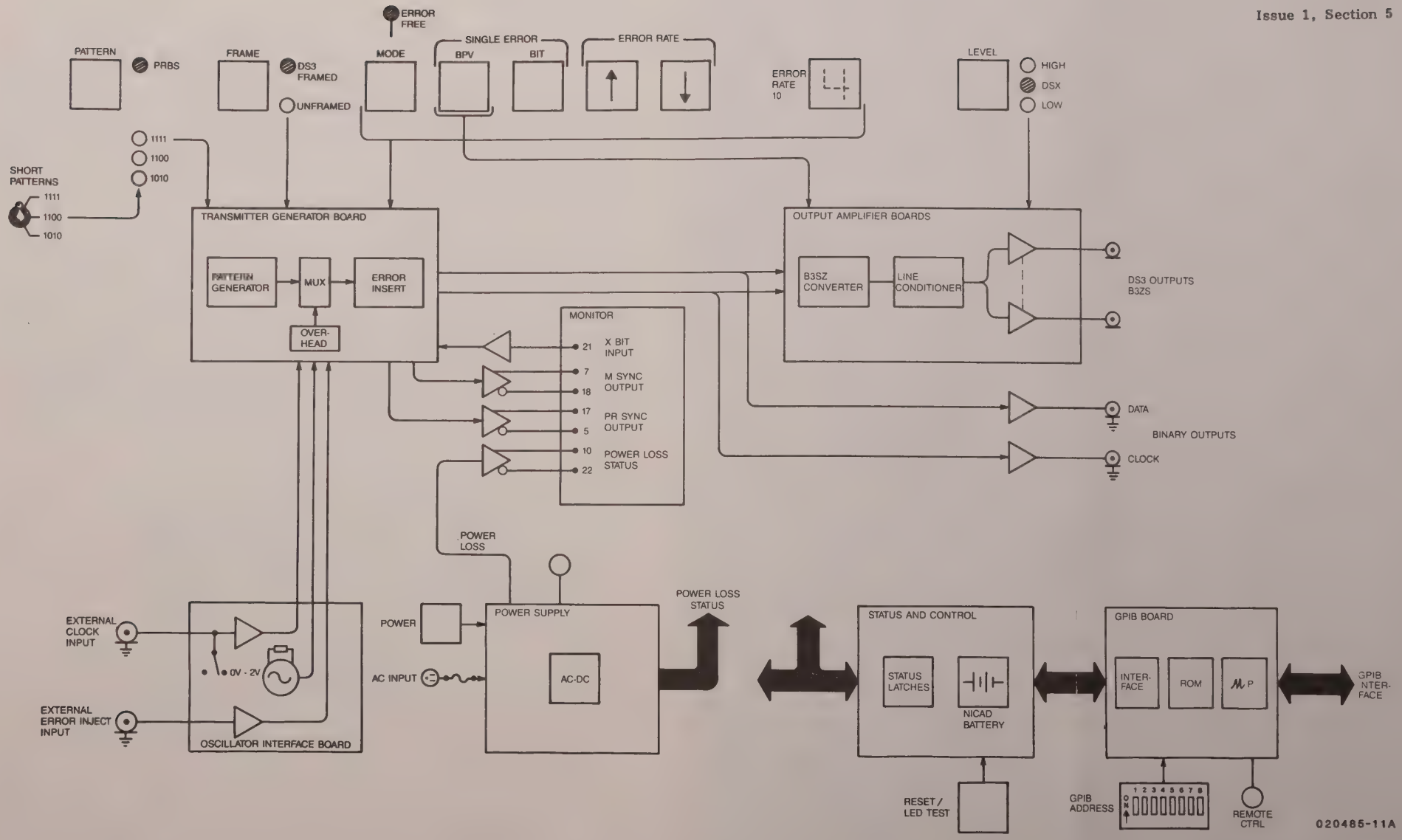


Fig. 6 - Transmitter System Functional Block Diagram

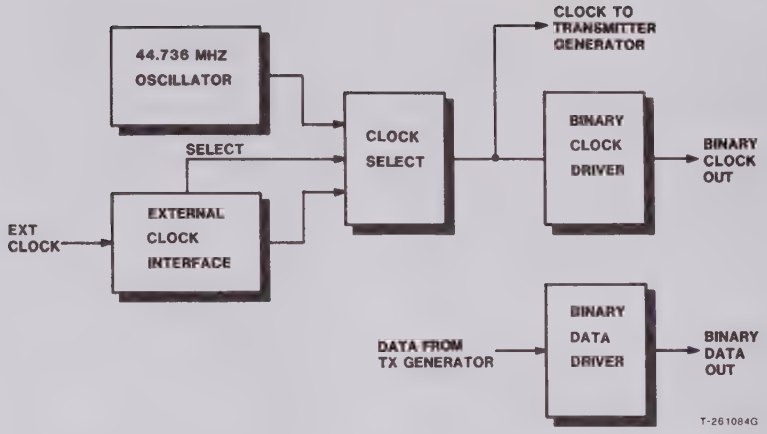


Fig. 7 - Oscillator Interface Board Functional Block Diagram

Transmit Generator Board

5.09 The Transmit Generator board (see Fig. 8) generates the DS3 master-frame data format and the $2^{15}-1$ (32,767) bit pseudorandom sequence for bit-error measurements. The board controls both the framed and unframed modes of operation, the insertion of bit errors in the output data format, the pseudorandom sequence, the short patterns (1111, 1100, 1010), and insertion of the BLUE signal.

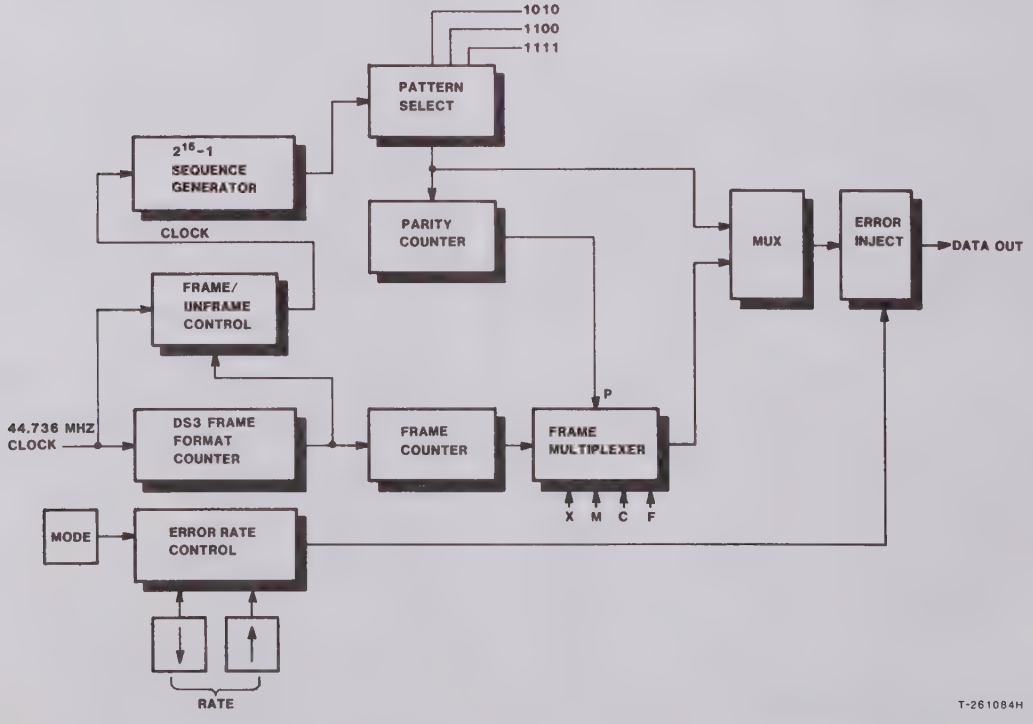


Fig. 8 - Transmit Generator Board Functional Block Diagram

5.10 In the unframed mode of operation, the information bits are transmitted without insertion of the DS3 master-frame format. The pseudorandom sequence and the short patterns can be transmitted in the unframed mode of operation. They are selected by the front-panel PATTERN pushbutton and the rear-panel SHORT PATTERNS switch.

5.11 In the framed mode of operation, the DS3 master-frame data bits are inserted into the information bits.

5.12 The DS3 format contains 4,760 bits per Master Frame, of which 56 are frame bits. The Transmit Generator generates the proper X, F, C, P, and M frame bits and inserts them into the data pattern.

5.13 A 44.2 MHz gapped clock is generated by the Transmit Generator board so that the pseudorandom sequence operates at the information bit rate. The frame bits are inserted during the gapped output of the sequence.

5.14 The Transmit Generator counts all the information bits in the Master Frame when the S5200E Transmitter is in the framed mode. If the digital sum of all 4,704 information bits is 1, the PP frame bits in the next Master Frame are 11. If the sum is 0, then PP is 00. These are the parity bits in the DS3 format that are used for measuring live traffic in a DS3 transmission system.

5.15 Circuitry in the Transmit Generator board allows the insertion of bit error-rates in the range of 10^{-2} to 10^{-9}. The range is set by the front-panel ERROR RATE pushbuttons. The errors are inserted in an asynchronous manner so that errors are applied to all bits within the 4,760-bit format. Therefore, errors are applied to the frame bits as well as the information bits.

5.16 A BLUE signal can only be generated in the framed mode of operation. It is defined as a 1010 pattern with DS3 framed bits inserted.

5.17 The Transmit Generator board also generates the PR-Sync and the M-Sync pulses. The PR-Sync pulse occurs once every 32,767-bit pseudorandom sequence. The M-Sync pulse occurs once every 4,760-bit DS3 Master Frame.

Output Amplifier Board

5.18 The Output Amplifier board (see Fig. 9) converts the NRZ data to a B3ZS format, sets the output level of the signal, and inserts single bipolar-pulse-violations in the B3ZS output when the front-panel SINGLE ERROR BPV pushbutton is pressed.

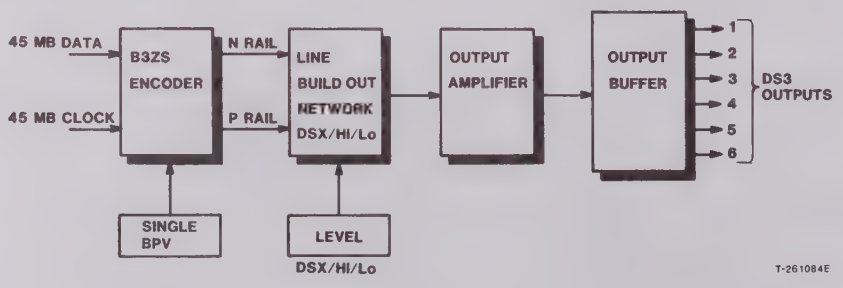


Fig. 9 - Output Amplifier Board Functional Block Diagram

5.19 The binary NRZ data and the timing information from the Transmit Generator board are applied to the B3ZS encoder on the Output Amplifier board. Two RZ rails are generated by the B3ZS encoder, a P rail and an N rail. These two rails are combined and amplified, sent through a pulse amplifier, and applied to a line-build-out network. There are three sections of this network: HIGH, DSX, and LOW. They are selected by the front-panel LEVEL pushbutton. DSX builds out 450 feet (137m) of cable; HIGH is straight thru, and LOW builds out 13.8 dB pad. The output of the amplitude and line-build-out network is fed to an output driver that drives six output buffers, each of which is connected to one of the six DS3 OUTPUT jacks on the front panel.

STD Interface Board

5.20 The STD Interface board (see Fig. 10) provides 1-of-2 switching between GPIB software control of the S5200E Transmitter and local front-panel control.

5.21 If the S5200E does not have the GPIB option installed, the 1-of-2 switching is disabled and the unit is operated by the normal local front-panel control.

5.22 With the GPIB option installed, when a GPIB controller has requested remote control of the Transmitter, all front-panel control inputs are switched out and the software control inputs are switched in. A partial STD bus interface allows the CPU board to issue transmitter commands and read transmitter status. Front-panel inputs are conveyed to this board by a flat ribbon cable interface from the front-panel printed circuit assembly. Transmitter control outputs from the STD Interface board are conveyed to the Transmit Generator and the Oscillator Interface boards by a non-standard transmitter control and status bus. Status inputs from these boards and the rear panel are provided over this same bus.

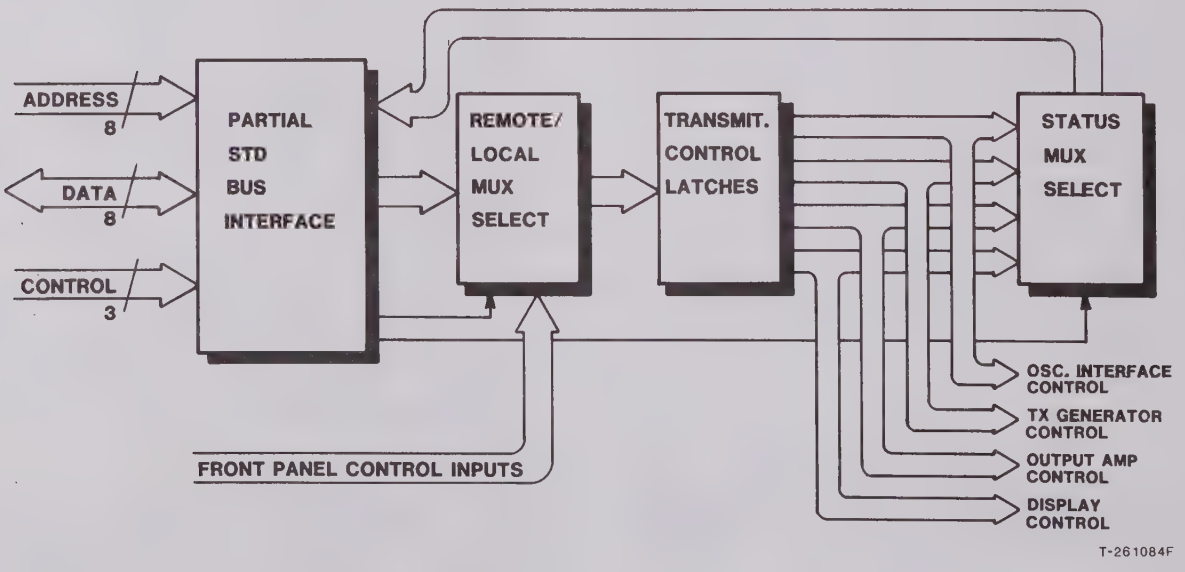


Fig. 10 - STD Interface Board Functional Block Diagram

GPIB Board

5.23 The GPIB board (see Fig. 11) provides an interface between the STD bus and the IEEE-488 interface. Most of the interfacing is handled automatically by an Intel 40-pin LSI device. GPIB activity causes status bits to be set in this IC which generates an interrupt to alert the CPU that something has happened. The CPU reads status and data from the GPIB IC and determines what software action to take.

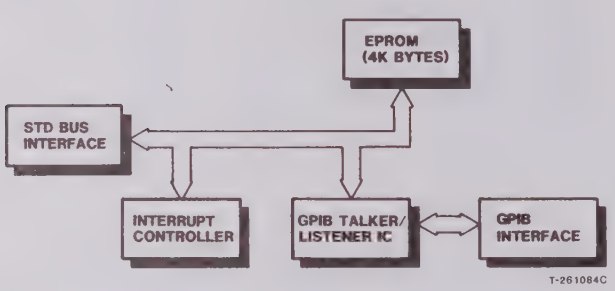


Fig. 11 - GPIB Board Functional Block Diagram

5.24 When GPIB commands are received by the GPIB board and processed by the CPU, the CPU writes the output to the GPIB IC. The GPIB IC controls the output on a byte-by-byte basis.

CPU Board

5.25 The CPU board (see Fig. 12) contains a Z80 microprocessor, 2K (2,048) bytes of volatile static RAM, and the interface circuitry with the 56-pin STD bus.

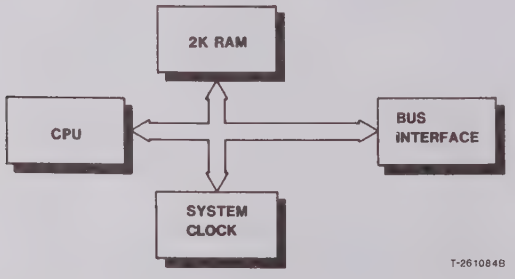


Fig. 12 - CPU Board Functional Block Diagram

5.26 The Z80 microprocessor is a 40-pin LSI device capable of addressing 65K bytes of memory and 256 I/O ports. The microprocessor operates on 8-bit parallel data.

5.27 The 2,084 bytes of RAM provide read/write storage for transmitter software variables and stack operations. Included in this RAM is a 512 byte GPIB output queue and a 128 GPIB input command buffer.

Front-Panel Display Board

5.28 The Front-Panel Display board (see Fig. 13) consists of push-button controls, LED's, and circuitry to interface these controls and LED's to the plug-in circuit boards as well as to control the functions and display the status of the transmitter.

5.29 All pushbuttons go through a switch debounce circuit. Therefore, when any pushbutton is pressed, a single pulse is generated.

5.30 The LEVEL pushbutton output drives a divide-by-3 counter which generates two outputs to control the transmit levels: DSX, HIGH, and LOW.

5.31 The FRAME and PATTERN push-buttons drive a divide-by-2 circuit whose output is fed to the STD Interface board, where it controls the FRAME and PATTERN select functions.

5.32 The MODE pushbutton output drives a divide-by-3 counter which has three outputs to control the ERROR FREE, ERROR RATE, and EXTERNAL ERR INJECT modes of operation.

5.33 The ERROR RATE up and down pushbuttons control a BCD up/down counter on the Front-Panel Display board. When the down push-button is pressed, the counter counts up to indicate a lower bit error-rate. Pressing the up pushbutton causes the

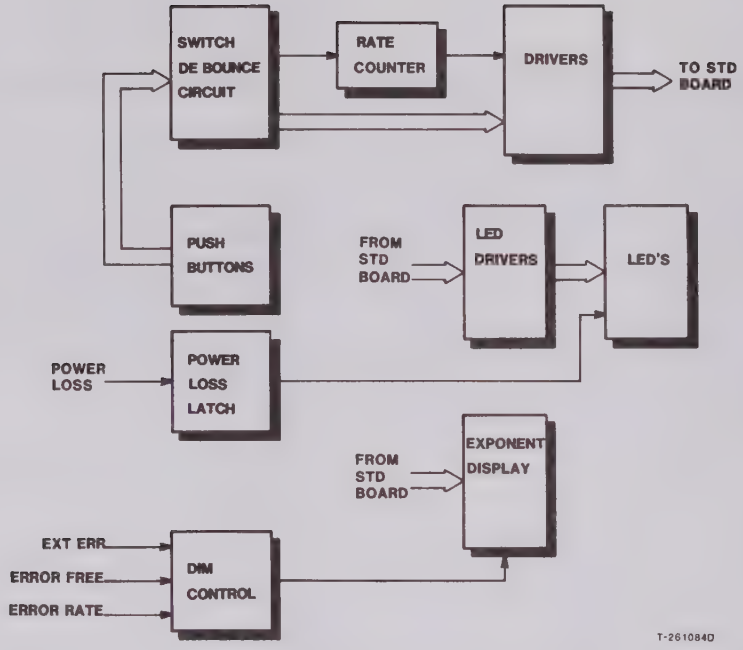


Fig. 13 - Front Panel Display Board Functional Block Diagram

counter to count down to indicate a higher bit error-rate. The BDC outputs of the counter are fed through the STD Interface board to the Transmit Generator board where it controls the insertion of errors into the output data.

5.34 The SINGLE ERROR BPV and BIT pushbutton outputs feed through the STD Interface board to the Transmit Generator board to control the single error insertion.

5.35 When power is lost and regained, the loss latch is set and turns on the POWER LOSS indicator. The latch is reset by the RESET/LED TEST Pushbutton.

C. Software Theory of Operation

5.36 The IEEE-488 (GPIB) option provides two software control functions: power-up self-test and GPIB remote control.

Power-Up Self-Test

5.37 On power-up, the software takes control very briefly to perform a basic self-test. All system RAM, program ROM, and remote/local switching control are tested. If any failures are detected during this self-test, a failure code is displayed for 5 seconds in the ERROR RATE LED. See Section 6E Software Diagnostics for a list and explanation of failure codes.

5.38 After the 5-second failure-code display, the software will again attempt a reinitialization and self-test. If the failure persists, the software will repeat this cycle until the failure is rectified.

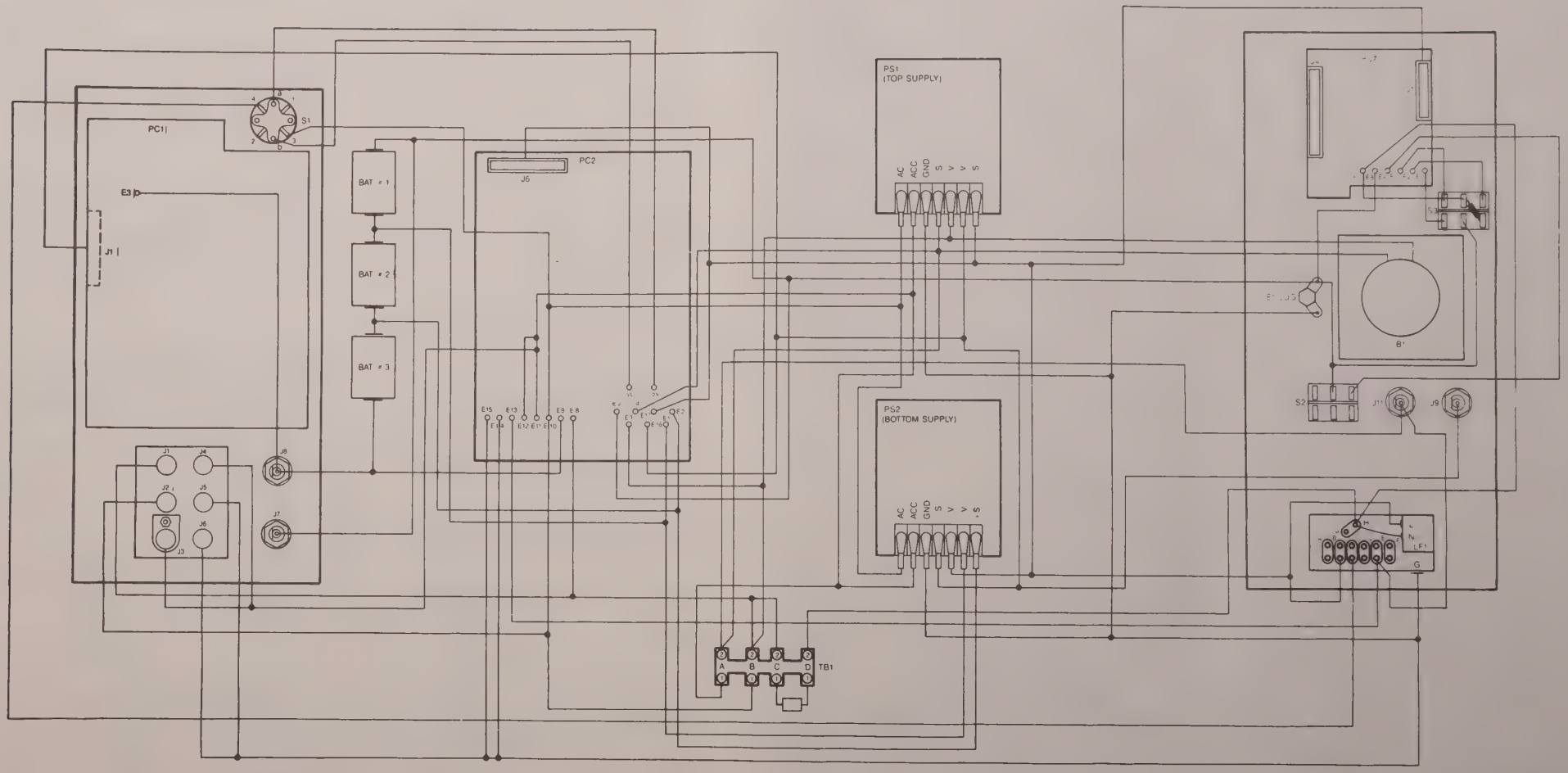
5.39 If no failures are detected, the self-test will end in less than 2 seconds, and the S5200E Transmitter is initialized under local front-panel control.

GPIB Control

5.40 The reception of GPIB commands "alerts" the software. When the transmitter is commanded via remote control by the GPIB, the software takes control of the transmitter functions. GPIB control software interprets incoming commands and outputs appropriate transmitter hardware control signals. Query commands cause the software to read transmitter hardware status and format ASCII output messages. These messages output to the GPIB hardware one character at a time.

D. Power Distribution

5.41 The S5200E Transmitter converts a 115 VAC power source to 5 Vdc for internal power distribution. The voltage is converted and distributed by two power supplies inside the Transmitter: a +5 V 12-amp power supply and a -5.2V 6-amp power supply. Figure 14 illustrates the power distribution of the Transmitter.



020485-11B

Fig. 14 - S5200E Transmitter Power Distribution

SECTION 6

SERVICE AND MAINTENANCE

6. SERVICE AND MAINTENANCE

A. Assistance

6.01 For service assistance, call the Tau-tron Customer Service Dept., (617) 692-5100 or 1-800-TAU-TRON. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

B. Repair Returns

6.02 If it is determined that the S5200E Transmitter must be returned to the factory for repair, use the Repair Return Card at the back of this manual and follow the directions to insure prompt service.

C. Routine Service

6.03 The fan air filter on the S5200E Transmitter rear panel must be vacuumed periodically. The dustier the working environment is, the more frequently this task must be performed.

Use the following procedure to clean the air filter:

STEP	PROCEDURE
1.	Remove the two screws from the filter holder, and remove the holder and sponge-rubber filter.
2.	Use a vacuum cleaner to clean the air filter.
3.	Reinstall the filter and holder and secure with the two screws.

WARNING: Failure to keep the fan air filter clean may result in overheating of the S5200E Transmitter, causing damage to the unit.

6.04 Other than occasionally cleaning the exterior surface with a mild cleaner, no other periodic maintenance of the Transmitter is required.

D. General Troubleshooting

WARNING: Do not attempt access to the inner printed circuit boards without disconnecting the line cord from the power receptacle.

Printed Circuit Boards

6.05 Printed circuit boards (PCB's) may have loosened in the sockets or ribbon cables may have disconnected. If so, perform the following:

STEP	PROCEDURE
1.	Remove the top enclosure to get access to the PCB's in the Transmitter.
2.	Be sure all PCB's are properly seated in the motherboard connectors.
3.	Be sure all interconnecting ribbon cables are properly secured to the PCB's.
4.	Replace the top enclosure removed in step 1.

Power Supply Voltage Test

6.06 Figure 15 illustrates the test points to check the internal power supply voltages. The voltages should be +5V ±0.2V and -5.2V ±0.2V.

6.07 Three 1.2V Nickel Cadmium batteries are used in the Transmitter to preserve front-panel settings in case of a power failure. The battery

is used to retain and remember the front-panel settings during a power failure. If the battery is discharged or disconnected, the front panel power up conditions will be incorrect. Figure 15 shows the location of the batteries. The batteries are C-size.

E. Software Diagnostics

6.08 When the Transmitter is equipped with the IEEE-488 Interface, software briefly takes control at power up to perform a basic self-test. All system RAM, program PROM, and remote/local switching control is tested. If any failures are detected during this self-test, a flashing failure code is displayed for 5 seconds in the ERROR RATE LED.

6.09 After the 5-second failure-code display, the software will again attempt a reinitialization and self-test. If the failure persists, the software will repeat this cycle continuously. If this occurs, call the factory. Under these conditions, the S5200E Transmitter cannot be remotely controlled.

6.10 If no failures are found, the self-test ends in less than 2 seconds and the S5200E Transmitter is initialized under local front-panel control.

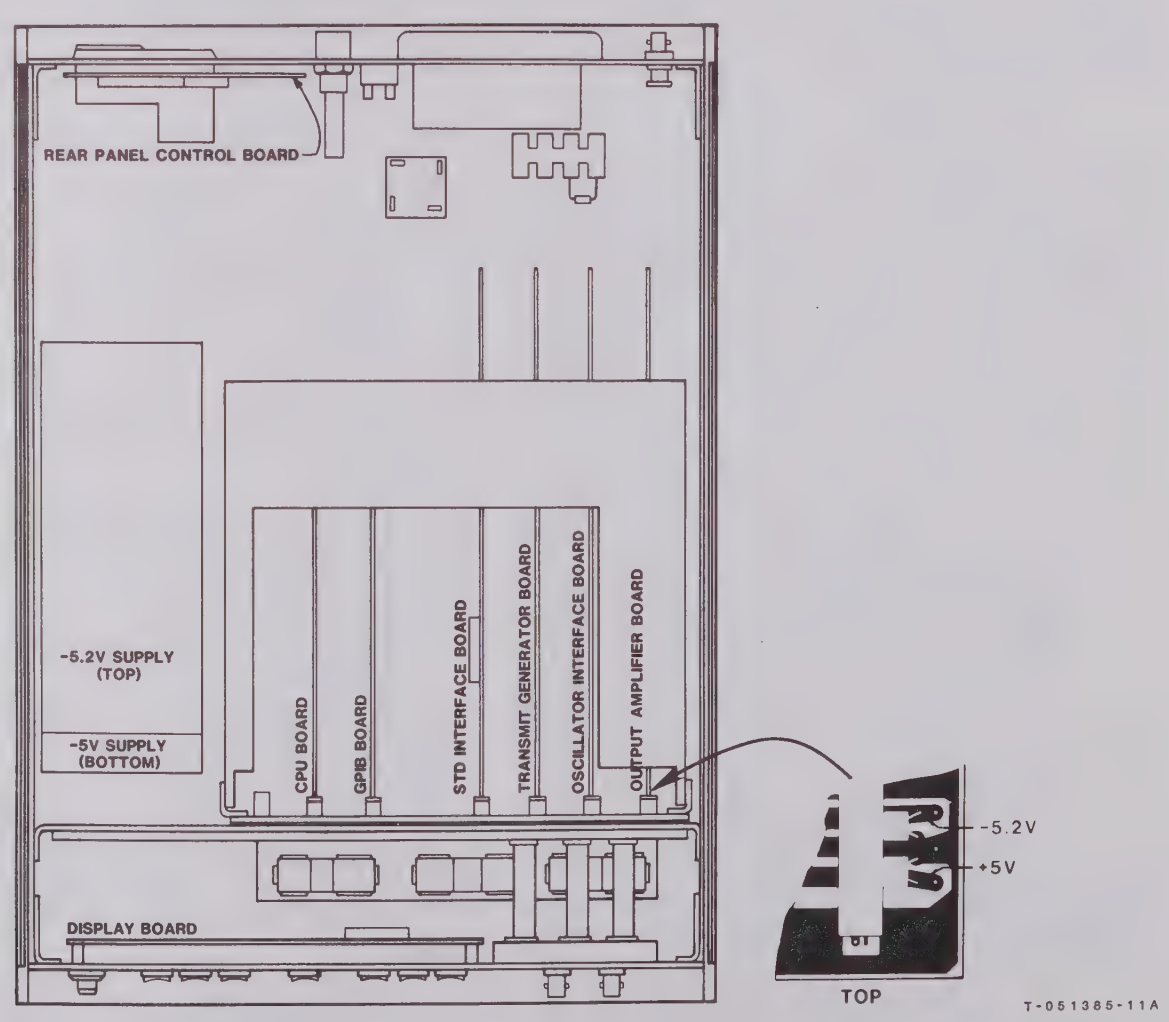


Fig. 15 - Power Supply Voltage Test Points and Nickel Cadmium Battery Location

APPENDIX A

DS3 TESTING

APPENDIX A DS3 TESTING

A. General

A.01 This appendix explains the DS3 Testing function of the S5200E. The following information is emphasized:

- DS3 Signal Format
- Parity Error Testing
- Frame Error Testing
- Bit Error Testing
- System Characterization using Error Seconds.

B. DS3 Signal Format

A.02 The 44.736 Mb/s DS3 signal format generated by the S5200E, MX3, and other multiplexers provide the basis for all DS3 framed measurements. Parity measurements on live traffic signals are made utilizing the DS3 format, as shown in Fig. 16.

A.03 There are seven subframes in the Master, or M Frame. Each subframe consists of eight groups of one housekeeping bit and 84 information bits.

A.04 The groups of 84 information bits can consist of sequences such as pseudorandom bit sequences (PRBS), short repeating bit sequences generated by test sets, system information such as live traffic, or patterns such as "Blue Signal" codes. When live traffic is being transmitted, the 84 data bits consist of 7 DS2 signals sampled 12 times. The 6.312 Mb/s DS2 signal is made of four 1.544 Mb/s DS1 signals. The DS1 signal can contain 24 PCM encoded voice channels. Therefore, a complete DS3 signal can contain 24 X 4 X 7 = 672 voice channels.

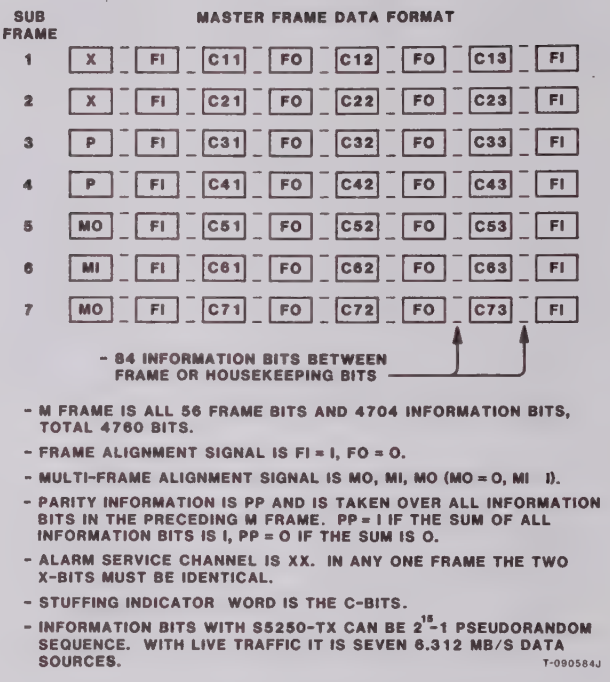

SUB FRAME
MASTER FRAME DATA FORMAT
1 X FI C11 FO C12 FO C13 FI
2 X FI C21 FO C22 FO C23 FI
3 P FI C31 FO C32 FO C33 FI
4 P FI C41 FO C42 FO C43 FI
5 MO FI C51 FO C52 FO C53 FI
6 MI FI C61 FO C62 FO C63 FI
7 MO FI C71 FO C72 FO C73 FI
- 84 INFORMATION BITS BETWEEN FRAME OR HOUSEKEEPING BITS
- M FRAME IS ALL 56 FRAME BITS AND 4704 INFORMATION BITS, TOTAL 4760 BITS.
- FRAME ALIGNMENT SIGNAL IS FI = I, FO = O.
- MULTI-FRAME ALIGNMENT SIGNAL IS MO, MI, MO (MO = O, MI I).
- PARITY INFORMATION IS PP AND IS TAKEN OVER ALL INFORMATION BITS IN THE PRECEDING M FRAME. PP = I IF THE SUM OF ALL INFORMATION BITS IS I, PP = O IF THE SUM IS O.
- ALARM SERVICE CHANNEL IS XX. IN ANY ONE FRAME THE TWO X-BITS MUST BE IDENTICAL.
- STUFFING INDICATOR WORD IS THE C-BITS.
- INFORMATION BITS WITH S5250-TX CAN BE 2^{15}-1 PSEUDORANDOM SEQUENCE. WITH LIVE TRAFFIC IT IS SEVEN 6.312 MB/S DATA SOURCES.
T-090584J

Fig. 16 - DS3 Signal Format

A.05 The DS3 housekeeping bits occur once every 85 bits and serve a variety of purposes. The 2nd, 4th, 6th, and 8th housekeeping bit in each subframe is termed the F-bit, or Frame Alignment signal. This 4-bit sequence of F1, F0, F0, F1 = 1001 is identical for each subframe. This known, repeating sequence is searched for and located by demultiplexing or test equipment so that the positions of other 84 information bits and housekeeping bits can be determined.

A.06 Demultiplexing or test equipment circuitry then must locate the seven subframes. The Marker bits, or M bits, are a sequence of M0, M1, M0 = 010 in the 5th, 6th, and 7th subframe of each Master Frame that serves this purpose. The method of locating the F and M bits is determined by the framing algorithm used in the communications equipment and is an important para-

meter in any system. The time to acquire DS3 Frame Synchronization depends on the algorithm used, and typically takes two to three milliseconds.

A.07 Once the subframes are located, the seven stuffing indicator words corresponding to the seven multiplexed DS2 channels are known. These 3-bit words (C11, C12, and C13 in Subframe 1) are always all zeros, or all ones, indicating the absence or presence of stuffing bits necessary for the asynchronous multiplexing of the DS2 channels.

A.08 Subframe location also defines the Parity (or P-bit and X-bit locations). The P bits in a Master Frame are used to provide a measure of error performance in the previous Master Frame. If the digital module-2 sum of all 7 x 8 x 84 = 4,704 information bits in a Master Frame is 1, then PP = 11 is output by the multiplexing or transmitting equipment in the next Master Frame. If the sum is 0, then PP = 00 is output. The demultiplexing equipment or test set receiver counts the 4,704 information bits in the Master Frame and compares this sum to the PP bits in the incoming format. If a transmission error has occurred in the information bits, the PP will not compare. The parity bits can be used to detect transmission errors in live traffic. However, if the error rate is such that double or even numbers of errors occur in a Master Frame, the parity error measuring becomes invalid. This occurs at error rates greater than $1/4{,}704 = 2.1 \times 10^{-4}$.

C. Parity Error Testing

Use

A.09 The parity-error mode is used to measure live traffic on standard data format DS3 signals generated by MX3 or M13 multiplexers (see Fig. 17). Parity measurements can be made on single hops or multi-hops if the parity is not restored at each repeater in the multi-hop system.

Parity Code

A.10 The multiplexer counts all the information bits in one Master Frame of 4,760 bits (see Fig. 16). If the digital sum of all 4,704 information bits is 1, then PP = 11 in the next Master Frame. If the sum is 0, then PP = 00 in the next Master Frame.

Parity Measurement

A.11 The S5200E Receiver monitors the DS3 signal at the receive end of the transmission system, finds the frame, and counts all of the 4,704 information bits in the Master Frame. It then compares the digital sum to the PP bits in the incoming format and, if they do not agree, generates a parity error.

Even Number of Errors

A.12 At the transmitter, if the digital sum is 1 and one bit error is made in one detected Master Frame during transmission, the digital sum at the receiver will be 0 for that Master Frame, and one parity error will be generated. Any odd number of bit errors (1, 3, 5, etc.) made in one Master Frame during transmission will be detected at the Receiver as one parity error. Any even number of bit errors (2, 4, 6, etc.) made in one Master Frame during transmission will not be detected at the Receiver.

Parity Errors vs. Bit Errors

A.13 The even/odd information from one frame is stored and compared to the parity bit received in the next frame. A difference indicates at least one data bit was in error. In general, the parity error rate will track the bit error rate, but is limited to representing one data bit error in a frame (1

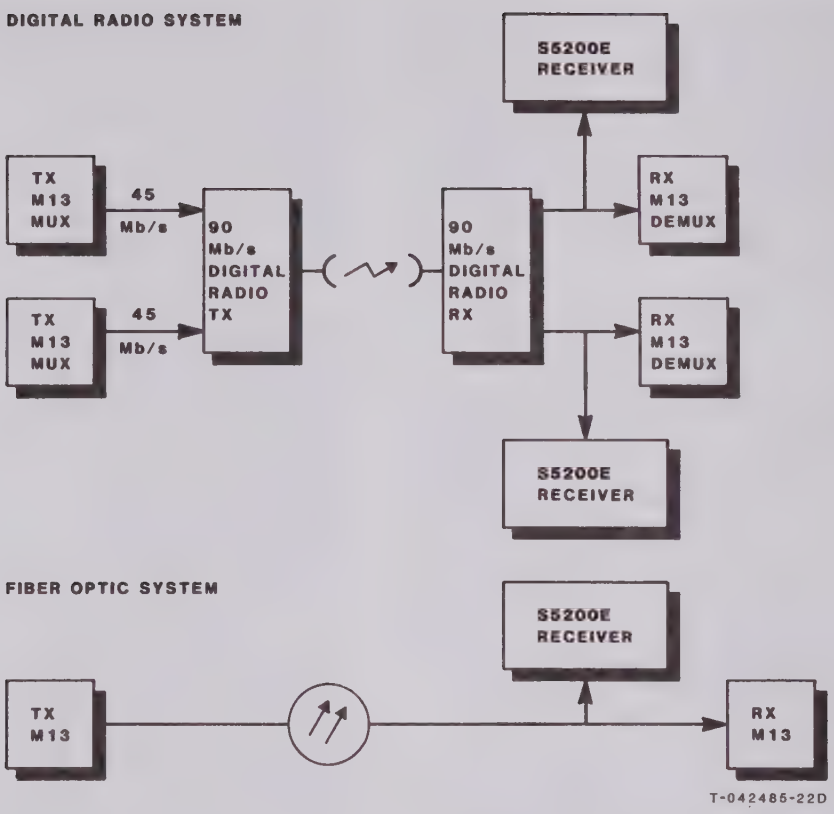


Fig. 17 - System Testing for Parity Errors

error bit divided by 4,704 data bits = 2.1×10^{-4} error rate). For error rates greater than this, bit errors will often be greater than parity errors.

Error Multiplication Factor

A.14 Most designers of digital systems use scramblers and descramblers and/or modulation schemes that cause a multiplication effect. This effect may result in three or more received errors from a single transmitted error. Fortunately, the error multiplication effect typically is contained within the 4,704-bit frame. Usually, system designers have made assurances that a statistically defined number of odd error sequences will occur so that the parity will still reflect bit errors. System manufacturers can supply the error multiplication factor for any particular system to allow the effective bit error rate to be determined by measuring the parity error rate.

D. Frame Error Testing

A.15 The frame-error mode is used to measure live traffic on standard data format DS3 signals generated by MX3 or M13 multiplexers (see fig. 17). Generally, parity measurements can be made on single hops or multi-hops if the parity is not restored at each repeater in the multi-hop system. Most multi-hop systems that restore parity do not generally restore or correct the frame, F1 and F0, bits. For these systems, frame error measurements may be the only way to detect system errors on live traffic. Also, for systems with error rates exceeding 2.1×10^{-4} error rate (the parity error measurement limit), frame error measurements provide an accurate way to determine error rate.

A.16 There are only 28 frame alignment bits (F1 and F0) in a Master Frame, as compared to the 4,704 information bits used in a parity measurement. Therefore, longer measurement times are required for frame measurements to achieve the same statistical accuracy as a parity measurement.

E. Bit Error Testing

Use

A.17 Bit error measurements are usually made during the initial installation of digital transmission systems (see Fig. 18). They are made using either the 2^{15}-1 (32,767) bit pseudorandom (PRBS) pattern, or short patterns generated by a S5200E Transmitter. Bit measurements can be made in the framed or unframed mode, depending on the system requirements.

Test Patterns

A.18 Bit error test equipment utilizes pseudorandom binary sequences or short patterns as the test pattern. The PRBS sequences are generated using digital shift register techniques. Their properties are such that the patterns appear to be random in nature because the density of 1's and 0's on the sequence are approximately equal. Another characteristic of these sequences is that they repeat after some number of bits. The length of the sequence in terms of its number of bits is 2^N-1, where N is the number of stages in the shift register generating the sequence. For the S5200E, N equals 15. Therefore, the length of the pseudorandom binary sequence before it repeats is 32,767 bits. Since the sequences repeat, it is easy to synchronize an incoming sequence received by a Receiver with a locally generated version of the same sequence.

Bit Measurements

A.19 The S5200E Transmitter output is applied to the transmit end of the system, and the S5200E Receiver input is connected to the receive end. The receiver synchronizes to the incoming pattern and compares it, bit by bit, to its own internal pseudorandom generator reference pattern. Any difference is counted as an error.

A.20 For systems not carrying live traffic, bit error measurements provide the most accurate assessment of system performance. With bit testing, several configurations are possible. Some parts of the systems do not require the DS3 format to operate properly. Inputs and outputs to some digital radio and fiber optic systems often only require the 44.736 Mb/s DS3 rate and do not require framing bits. For these situations, it may be desirable to utilize the unframed mode of the test set to eliminate the DS3 frame acquisition time of the receiver. For example, short patterns can be used in bit testing, and a comparison of system performance between pseudorandom and short patterns can often be used on some systems to detect misalignment problems or timing recovery problems.

F. Bipolar-Pulse-Violation (BPV) Testing

A.21 Bipolar-Pulse-Violation (BPV) testing is valid for live traffic testing of cable systems and entrance links even though this type of testing has limited usefulness for DS3 systems.

A.22 The DS3 signal has a bipolar signal format. This means that all binary logical zeros are transmitted as a 0V signal, and all binary logical ones are transmitted as positive or negative pulses of widths equal to one-half the clock period. Bipolar coding requires that these pulses alternate in polarity. A noise impulse on a cable system or entrance link may cause a 0V logical zero to be recognized as a bipolar pulse or may cause a legitimate bipolar pulse to be recognized as a 0V logical zero. Either impairment will result in received bipolar pulses

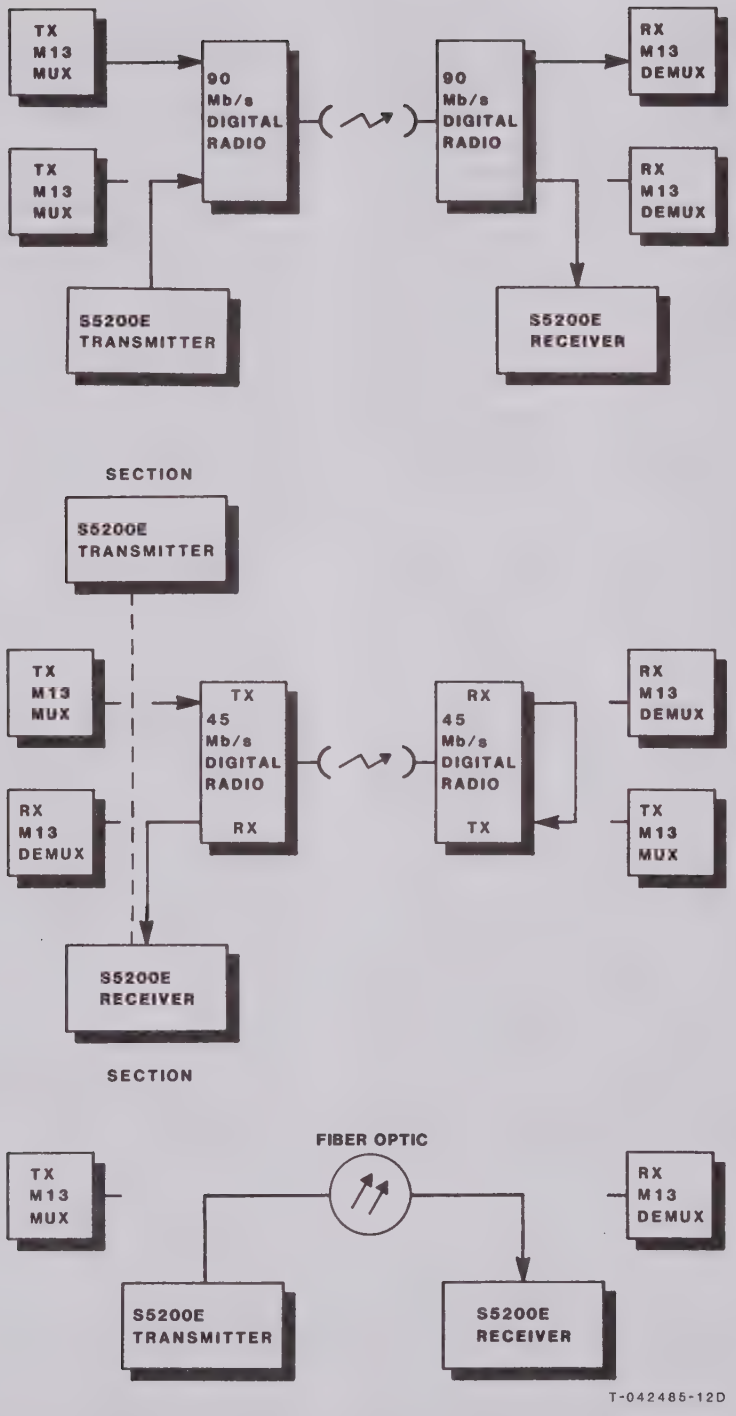


Fig. 18 - System Testing for Bit Errors

that do not alternate in polarity, but are of the same polarity. Therefore, a performance determination can be made on a signal with a bipolar format without regard for content or framing format.

A.23 The DS3 signal coding also requires a Bipolar 3 Zero Substitution (B3ZS) code. When three zeros are present in the binary data, substitution codes consisting, in part, of a bipolar violation are transmitted instead. The codes are varied to maintain the 0V average DC level of the bipolar signal and are transmitted to guarantee activity on the line as some minimal activity is a requirement of some regenerative repeaters and DS3 terminating equipment. This B3ZS coding makes BPV error measurements slightly more complex in that legitimate violation codes are not recorded as errors.

A.24 The S5200E Receiver is excellent for BPV error measurements with its high input sensitivity and cable equalization optimized for 450 to 900 feet of 728A cable. However, BPV measurements of the DS3 signal have limited usefulness. Since the DS3 format includes a parity check, live traffic parity measurements are usually used. When bipolar pulses are passed through digital processing circuitry, the bipolar pulses are converted to binary logic levels and then processed. When these binary levels are then converted back to bipolar signals, any input bipolar violations are lost and not retransmitted. Therefore, BPV measurements can only be used to test a single section of a system. Where the DS3 framing format is available, parity measurements often provide useful results.

G. System Characterization Using Error Seconds

Synchronous Error Seconds

A.25 The error second is one measurement accepted as an indicator of performance. It is defined as a one-second period in which there are one or more errors. Specified limits for error seconds are required for some systems. Error seconds have been used to compare systems and evaluate the effects of various parameters on system performance.

A.26 In some instances the error-second measurement has been quantified by its severity. That is, if an error second occurs in which the errors exceed a specified rate, then it is recorded as a threshold error second. For example, in voice grade PCM systems, error-rates exceeding 10^{-6} error bits are sometimes of interest because the error perturbations become noticeable at this error-rate. At 10^{-3} error-rates, voice quality becomes unacceptable. As a result, 10^{-6} and 10^{-3} threshold error seconds would be useful for assessing performance of systems accommodating voice PCM signals.

A.27 Two types of error-second measurements are in general use, synchronous and asynchronous (see Fig. 19).

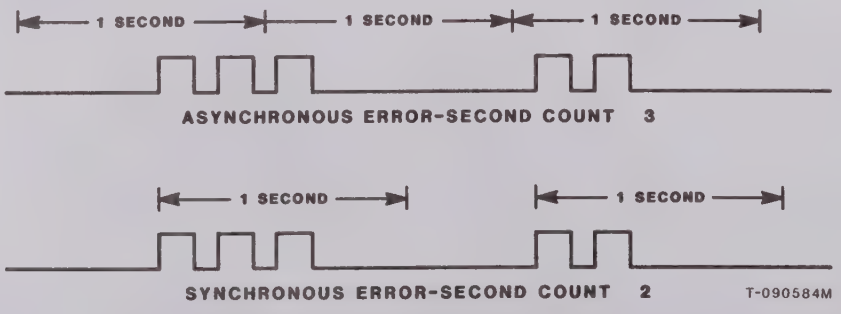


Fig. 19 - Synchronous and Asynchronous Error-Second Format

A.28 With asynchronous measurements, contiguous one-second measurements are made starting at some time independent of the errors. Any error or errors occurring during any one-second interval registers as an error second. With synchronous measurements, the one-second measurements are triggered by the errors.

A.29 Synchronous error-second measurements always give the lowest possible count and always give consistent counts. Two test sets making the same measurement will always read the same. For these reasons, synchronous error-second measurements are used by Tau-tron and are preferred by industry.

System Characterization

A.30 Many digital systems can be characterized as having a combination of randomly distributed, infrequent, or dribbling type errors and occasional error bursts. While all errors contribute to the overall or average error-rate of a system, the causes of burst and dribbling errors are often quite different. Quantifying these different types of errors and correlating them with other parameters can be very useful in determining their causes. Error bursts are caused by many things from power surges and propagation phenomena to intermittent connections and slamming doors, while dribbling type errors can often be related to system distortions, circuit misalignments, and other more subtle problems.

A.31 Dribbling errors, or errors that occur infrequently, can be related to a system's error-rate "floor." This floor can be described as the best or lowest error-rate that a system achieves over a long period of time. Systems operating poorly may have a lower limit or error-rate floor of 1 error in 10^5 or 10^{-5} error-rate. Systems operating properly may run for days without errors and have error-rate floors of 10^{-13} or lower. In many cases the error-rate floor may be so low that it appears to be zero. The S5200E separates dribbling errors from other burst type errors and calculates a dribbling error-rate from these errors and the elapsed time of test to give an indication of the system's present error-rate floor. One approach to system maintenance and troubleshooting is to attack the burst type error first since they may tend to mask the lower level dribbling errors. The S5200E also quantifies the severity of the burst errors and provides a correlation between other system parameters to aid isolating cause and effect.

Threshold Error Seconds

A.32 Since the S5200E measures error seconds synchronously, it can accurately quantify the error distribution of a system by an extension of the synchronous error second to the synchronous threshold error second. A threshold error second is a second in which the error rate exceeds 10^{-3}, 10^{-4}, 10^{-5}, and 10^{-6}. In this way, a system can be characterized by the severity of error bursts that cause the specific thresholds to be exceeded. These specific error thresholds have been programmed into the solid-state memory of the S5200E. If the number of errors exceeds this threshold during an error second, then the appropriate threshold error-second totals are incremented.

Thresholds

A.33 The number of errors that causes a specific error-rate depends on the mode of operation. For example, bit error measurements in the unframed mode are made on a bit-by-bit basis over all bits in the 44.736×10^6 bit per second data stream. An error-rate worse than 10^{-3} would then require more than 44,736 errors a second. Bit measurements in the framed mode are

only made on the data bits and do not include the DS3 framing bits. The framing bits occur once every 85 bits; the effective data bit rate is 84/85 x 44.736 Mbs, or 44.210 Mbs. Therefore, for the framed mode, the number of bit errors must exceed 44,210 errors in a second to cause an error-rate worse than 10^{-3}.

A.34 Parity measurement thresholds are the same as DS3 framed bit measurements with the exception that since the parity bit represents 4,704 data bits in a DS3 Master Frame, the parity measurement cannot accurately detect error-rates worse than 1 error per 4,704 bits or 2.1×10^{-4}. Therefore, 10^{-3} threshold error seconds are invalid. A 10^{-4} threshold parity error second would require 4,421 or more errors a second.

A.35 The error-second thresholds in the S5200E have been set to consider the mode of operation, and have also been adjusted to take into account the accuracy of the internal crystal controlled timing circuit which generates the synchronous one second interval. The actual error thresholds for the specific threshold error seconds are shown in Table D. If these error thresholds are exceeded, then the appropriate threshold error-second counts are incremented in the S5200E.

Dribbling Errors

A.36 When errors occur during a second that does not exceed a 10^{-6} error-rate, they are termed dribbling or residual errors. The S5200E receiver maintains an exact totalized count of all dribbling errors and also calculates the dribbling error-rate, which can be related to a system error-rate floor. If this floor is unacceptable, then another level of trouble-shooting aimed at the causes of dribbling errors is required.

Event Seconds

A.37 To aid in cause and effect diagnosis, the S5200E accumulates the number of seconds when certain parameters have occurred. Signal loss, DS3 frame loss, data sync loss, Blue signal detected, DS3 X-bit logic low and four TTL compatible external events are monitored. Their occurrence is recorded in separate accumulators. This provides further insight into system performance and can be useful in determining the relation between signal status, external system parameters, and error performance, particularly when the S5200E printer output is used.

TABLE D

ERROR THRESHOLDS

ERROR THRESHOLDS IN ONE SECOND PERIOD			THRESHOLD ERROR RATE
DS3 Framed Bit, Parity Measurement	Unframed Bit Measurements	Frame Error Measurements	
44100	44700	260	1×10^{-3}
4410	4470	26	1×10^{-4}
441	447	2	1×10^{-5}
44	44	-	1×10^{-6}

APPENDIX B

IEEE-488 INTERFACE (GPIB)

IEEE-488 INTERFACE (GPIB)

A. General

B.01 This appendix provides an introduction to the GPIB (General Purpose Interface Bus) and explains the operation of the S5200E Transmitter under GPIB for those units with the IEEE-488 Interface option installed. The S5200E Transmitter may communicate with other GPIB compatible devices as a talker/listener or as a listener only.

B. Introduction

B.02 The GPIB transfers data and commands between the units of an instrumentation system on 16 lines. The interface functions for each unit are performed within the unit; therefore, only passive cabling is necessary to connect the system.

B.03 Eight of the lines, DI01 thru DI08, are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer are asynchronous and are coordinated by the 3 handshake lines: DAV (data valid), NRFD (not ready for data), and NDAC (not data accepted). The other 5 lines are for control of bus activity.

B.04 Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the roll of each of the other units by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DI01 thru DI08). Addresses are set into each device at the time of system configuration either by switches built into the unit or by jumpers on a printed circuit board. While the ATN line is true, all units must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

B.05 Several listeners can be active simultaneously, but only one talker can be active at a time. Whenever a talk address is put on the data lines, while ATN is true, all other talkers should be automatically unaddressed.

B.06 Information is transmitted on the data lines under sequential control of the 3 handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as units can respond, but no faster than allowed by the slowest device being addressed as active. This permits several devices to receive the same message byte concurrently.

B.07 The ATN is one of 5 control lines. When ATN is true, addresses and universal commands are transmitted on only 7 of the data lines using ASCII code. When ATN is false, any code of 8 bits or less understood by both the talker and listeners can be used.

B.08 The other control lines are: IFC, REN, SRQ, and EOI. IFC (interface clear) places the interface system in a quiescent state. REN (remote enable) is used with other coded messages to select either local or remote control of each unit.

B.09 Any active unit can set the SRQ (service request) line to true. This indicates to the controller that some unit on the bus wants attention; for example, a counter on a bus may want attention because it has just completed a time-interval measurement and wants to transmit the reading to a printer.

B.10 EOI (end or identify) is used by a unit to indicate the end of a multiple-byte transfer sequence. When a controller sets both ATN and EOI lines to true, each unit capable of a parallel poll indicates its current status on the data line (DI01 thru DI08) assigned to it.

B.11 It is not necessary that every unit be capable of responding to all lines. Each unit can be designed to respond only to those lines that are pertinent to its functions on the bus.

S5200E Transmitter GPIB Capabilities

B.12 The S5200E Transmitter may be interfaced as a talker/listener or as a listener only. The following GPIB capabilities, as described in the IEEE-488-1978 standard, are implemented:

- SH1 Complete source handshake
- AH1 Complete accepter handshake
- T6 Basic talker, serial poll, no talk only, unaddress if addressed to listen
- TEO No extended talker (secondary listen address) capability
- L3 Basic listener, listen only, unaddress if addressed to talk
- LEO No extended listener (secondary listen address) capability
- SR1 Complete service request capability
- RL2 No local lockout on remote/local capability
- PPO No parallel poll capability
- DC1 Complete device clear capability
- DT1 Complete device trigger capability
- CO No control capability
- E2 Tri-state drivers are used on DI0 lines to achieve maximum data transfer rates.

C. GPIB Interface Connections

B.13 A 24-pin GPIB connector is located on the rear panel of the S5200E Transmitter. The connector is mounted on all units, but is operational only on those units equipped with the IEEE-488 Interface option. Tri-state drivers are used on the DI0 lines in the talk mode to achieve higher data transfer rates.

GPIB Address and Option Selection

B.14 An 8-section DIP switch is located on the rear panel adjacent to the GPIB connector. It is used to select and set the GPIB talk/listen address. Table E and Figure 20 explains the DIP switch settings.

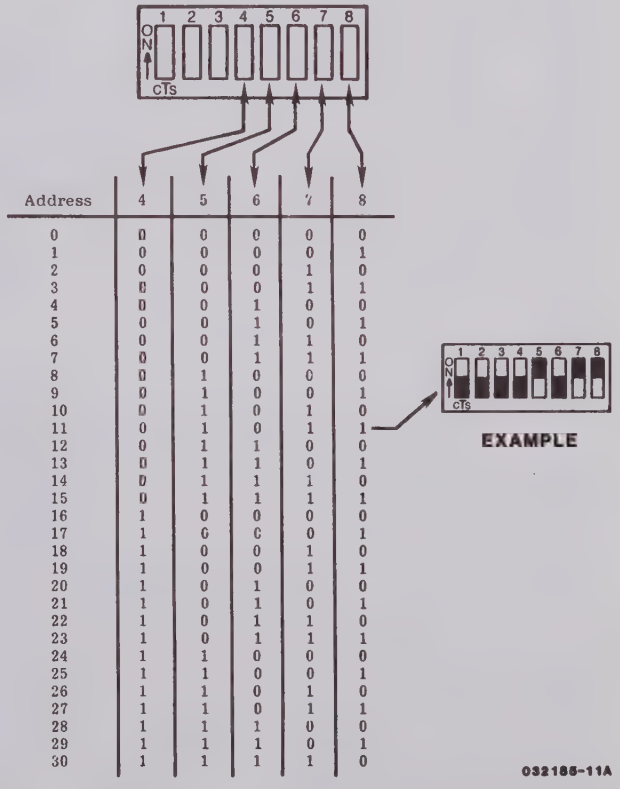


Fig. 20 - GPIB Address Dip Switch Setting

TABLE E

GPIB DIP SWITCH SETTINGS

SWITCH	FUNCTION	DESCRIPTION
1	SRQ Enable	When set to ON, the S5200E Transmitter is allowed to generate service requests (assert the GPIB SRQ line). In systems with many GPIB units, this may not be desirable. Service requests can be inhibited by setting this switch down to its off position. The S5200E Transmitter maintains status and will respond to serial polls regardless of the SRQ Enable setting.
2	Talk Only	This setting is ignored by the S5200E Transmitter as it does not have a talk-only mode.
3	Listen Only	When switched to ON, the S5200E Transmitter can be remotely controlled but cannot be addressed to talk.
4	Address A5	A1 thru A5 plus two additional bits, which are independent of the switch settings, form a 7-bit talk and listen address. A1 thru A5 are the least significant bits. The two additional bits are the most significant bits. They are fixed as 1-0 for a talk address and as 0-1 for a listen address. Once the 5 address bits A1 thru A5 are selected, both talk and listen addresses are specified for the receiver.
5	Address A4	
6	Address A3	
7	Address A2	
8	Address A1	

NOTE: The DIP switch settings are read on Power-Up only. To change the S5200E Transmitter's GPIB address or other characteristics, the Transmitter must be turned OFF, reset, and then turned ON.

D. S5200E Response To GPIB Commands

B.15 The S5200E Transmitter does not respond to all GPIB capabilities. The following is a list of commands and events that are supported by the S5200E Transmitter:

- S5200E TX addressed to listen (MLA)
- Universal unlisten command (UNL)
- S5200E TX addressed to talk (MTA)
- Data byte received (DBR)
- Remote/local command (REN)
- Device clear command (SDC,DCL)
- Device trigger command (GET)
- Serial poll enable/disable command (SPE,SPD).

B.16 Several GPIB capabilities are not supported by the S5200E Transmitter. The following commands are ignored:

- Local lockout
- Identify (parallel poll trigger)
- Secondary addresses
- Parallel poll configure/unconfigure
- Parallel poll enable/disable
- Take control.

B.17 The following paragraphs detail the GPIB commands and events to which the S5200E Transmitter will respond.

S5200E Transmitter Addressed to Listen

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
MLA	Y 0 1 L L L L L (5 4 3 2 1)	1 x x x x

L1-L5 specify the device dependent bits of the device's listen address as set by the rear-panel DIP switch.

B.18 When MLA (my listen address) is present on the GPIB bus, the S5200E Transmitter will be addressed to listen. The Transmitter will automatically untalk, if it was previously addressed to talk. The Transmitter cannot be configured to talk and listen at the same time. This is to prevent its talk data from being interpreted as commands.

Universal Unlisten Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
UNL	Y 0 1 1 1 1 1 1 1	1 x x x x

B.19 When UNL (unlisten) is present on the GPIB bus, the S5200E Transmitter will cease to listen and addressed commands (GET, GTL, and SDC) and data will be ignored. Universal commands (IFC, REN, DCL, SPE, SPD, MLA and MTA) will continue to be recognized and responded to.

S5200E Transmitter Addressed To Talk

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
MTA	Y 1 0 T T T T T (5 4 3 2 1)	1 x x x x

T1-T5 on the DIO lines specify the device dependent bits of the device's talk address as set by the rear-panel DIP switch.

B.20 When MTA (my talk address) is present on the GPIB bus, the S5200E Transmitter will be addressed to talk. If the Transmitter was previously addressed to listen, it will automatically unlisten to prevent output data from being interpreted as commands. Since a GPIB system can have only one talker, unique talk addresses must be selected for each device in the system. All other devices must untalk when the Transmitter is addressed to talk. If addressed to talk after SPE (serial poll enable) and before SPD (serial poll disable), the Transmitter will respond by putting its status byte on the DI0 lines (described later under the Service Request and Serial Poll Response section). Otherwise, Transmitter output data, i.e. status, will be placed on the DI0 lines. If the Transmitter has nothing to say, it will output one or two null bytes along with EOI.

Universal Untalk Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
UNT	Y 1 0 1 1 1 1 1	1 x x x x
OTA	OTA = SGA ∧ $\overline{\text{MTA}}$	

The UNT code is provided for system use.

B.21 The presence of the UNT (untalk) command or a talk address other than the S5200E Transmitter's OTA (other talk address) causes the Transmitter to become unaddressed to talk. If service requests are not inhibited and the Transmitter still has data it wishes to output, a service request, indicating request-to talk, will be generated.

B.22 When the GPIB ATN (attention) line is active, bytes received on the eight DIO lines will be interpreted as device-dependent commands (see Device-Dependent Commands).

Data Byte Received

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
ATN	x x x x x x x x	1 x x x x
DAB	D D D D D D D D 8 7 6 5 4 3 2 1	0 x x x x

D1-D8 specify the device dependent data bits.
The source of the message on the ATN line is always the C function, whereas the messages on the DIO and EIO lines are enabled by the T function.

B.23 When the GPIB ATN (attention) line is inactive and the S5200E Transmitter is addressed to listen, bytes received on the eight DI0 lines will be interpreted as device-dependent commands (see Device-Dependent Commands).

Interface Clear Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
IFC	x x x x x x x x	x x x 1 x

B.24 When the IFC (interface clear) line is asserted on the GPIB bus, the S5200E Transmitter reinitializes its interface functions as described by IEEE-488-1978 state diagrams. A pending service request will be cleared. However, the status byte in the transmitter is not cleared. It may be polled to determine if bus errors, indicated in the status byte, may have caused bus problems prior to the interface clear command. If in the remote mode, reception of the interface clear command does not return the S5200E Transmitter to local control.

Remote Local Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
GTL	Y 0 0 0 0 0 0 1	1 x x x x
LLO	Y 0 0 1 0 0 0 1	1 x x x x
REN	x x x x x x x x	x x x x 1

B.25 When the REN (remote enable) line is asserted on the bus and the S5200E Transmitter is addressed to listen, the Transmitter is put in remote mode. Since the Transmitter has no return-to-local front-panel control, local lockout capability is not provided. While in remote mode, all local control (front-panel pushbuttons) is disabled. The Transmitter may be remote-enabled only by first asserting the REN line under remote control. REN going inactive will return it to local control. If addressed to listen and in the remote mode, the presence of the GTL (go to local) message returns the Transmitter to local control. LLO (local lockout) is ignored at all times.

B.26 The Transmitter responds to commands issued by GPIB only when it is in the remote mode. Commands issued while the Transmitter is under local control are saved. When the S5200E Transmitter is put into the remote mode, previously issued GPIB commands take effect.

B.27 When the Transmitter is returned to local control, it returns to the mode previously selected by front-panel control. If any pushbuttons were pressed while the Transmitter was

under remote control, the Transmitter's mode reflects those pushbutton selections when returned to local control.

Device Clear Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
DCL	Y 0 0 1 0 1 0 0	1 x x x x
SDC	Y 0 0 0 0 1 0 0	1 x x x x

B.28 When under remote control, the S5200E Transmitter may be cleared by DCL (universal device clear) or SDC (selective device clear). SDC is accepted only if the S5200E Transmitter is currently addressed to listen. DCL is responded to whether addressed to listen or not, as long as the Transmitter is under remote control. In response to a device clear command, the Transmitter functions are returned to the following states:

- ERROR MODE = ERROR FREE
- ERROR RATE EXPONENT = 9
- FRAME MODE = FRAMED
- PATTERN = PRBS
- LEVEL = DSX

The Transmitter will remain under remote control, and the power loss history status will be cleared. The Transmitter's GPIB interface is not reinitialized. When the Transmitter is in the local mode, device clear causes the software to return to the status listed above. The Transmitter will not return to those states until it is put in the remote mode.

Device Trigger Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
GET	Y 0 0 0 1 0 0 0	1 x x x x

B.29 The S5200E Transmitter takes no action in response to GET (group execute trigger) being present on the bus.

Serial Poll Enable/Disable Command

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
SPD	Y 0 0 1 1 0 0 1	1 x x x x
SPE	Y 0 0 1 1 0 0 0	1 x x x x

B.30 The SPE (serial poll enable) and SPD (serial poll disable) commands are recognized by the S5200E Transmitter when they are present on the bus. In response to a serial poll, the Transmitter will put its GPIB status byte on the DI0 lines. The serial poll command sequence and status byte interpretation are described later under Service Request and Serial Poll Response.

Unsupported GPIB Commands

B.31 No parallel poll functions: IDY (identify), PPC (parallel poll), PPE (parallel poll enable), PPD (parallel poll disable), PPU (parallel poll unconfigure), and LLO (local lockout), or control functions TCT (take control) are supported by the S5200E Transmitter. The occurrence of these commands on the bus is ignored at all times. Undefined GPIB commands received with the ATN line asserted are also ignored.

E. Device Dependent Commands

B.32 All S5200E Transmitter capabilities controllable from the front panel may be remotely controlled. A set of device-dependent commands issued on the GPIB bus selects the S5200E Transmitter commands. When the Transmitter is addressed to listen, data accepted on the DI0 lines is interpreted as Transmitter commands.

B.33 Programming the Transmitter in remote control is as simple as programming it by front-panel entry. Nine commands correspond to the front-panel pushbuttons. Five additional commands are provided to return Transmitter status to the controller. Table F summarizes the device-dependent commands.

Command Sequence Formats

B.34 All device-dependent command sequences must be issued in the following format: Command 1 (delimiter, Command 2) (delimiter, Command 3)...CR LF Command 1, 2, 3, etc. are any of the mnemonics shown in Table F. Each character of the command sequence is read as a 7-bit ASCII code off the DI0 lines. Multiple commands in a command sequence must be delimited by any of the following valid delimiters. Every command sequence must be terminated by a carriage return or line feed.

Delimiter	ASCII Code (hex)
SP (blank).....	20
NULL (null byte).....	00
, (comma).....	2C
; (semicolon).....	3B
HT (tab).....	09

Command Errors

B.35 Invalid commands are ignored by the Transmitter. If a multiple command sequence contains an invalid command, valid commands in the sequence will still be interpreted and responded to. Invalid mnemonics cause the command error bit to be set in the Transmitter's serial poll status word. If service requests are enabled, command errors also generate a service request.

S5200E Transmitter Output To GPIB

B.36 Five output commands allow Transmitter status to be snapshot and queued for output to the bus. The format and function of these five commands are shown in Table F and described below. The output commands may be issued individually or in a sequence as described.

B.37 In response to the MD? command, the Transmitter error mode and remote/local status will be snapshot and a corresponding ASCII mnemonic queued for output to the bus. The error modes and corresponding mnemonics are as follows:

MODE	MNEMONIC
local, error free	LOCFRE
local, error rate insert	LOCINS
local, external error	LOCEXT
remote, error free	REMFRE
remote, error rate insert	REMINS
remote, external error	REMEXT

TABLE F

DEVICE-DEPENDENT COMMANDS

REMOTE COMMAND	CORRESPONDING KEY	FUNCTION
MD	MODE	Select error-free, error-rate inject, or external error inject.
DN	↓	Decrease error-rate (NOTE: error-rate of 10^{-3} decrease from 10^{-2}).
UP	↑	Increase error-rate.
BP	BPV	Inject single BPV error.
BI	BIT	Inject single BIT error.
RS	RESET/LED TEST	Reset power loss LED; does not perform LED test.
FR	FRAME	Select framed/unframed transmit mode.
PA	PATTERN	Select PRBS, 1111, 1100, or 1010 pattern.
LV	LEVEL	Select high/DSX/low signal level.
MD?	none	Snapshot transmitter mode.
RT?	none	Snapshot current error injection rate.
FR?	none	Snapshot current frame mode.
PA?	none	Snapshot current pattern.
LV?	none	Snapshot current transmit level.

B.38 In response to the RT? command, the Transmitter error insertion rate will be snapshot and queued for output to the bus. Error-rates and the output ASCII mnemonics are as follows:

ERROR RATE	MNEMONIC
10^{-9}	E-9
10^{-8}	E-8
10^{-7}	E-7
10^{-6}	E-6
10^{-5}	E-5
10^{-4}	E-4
10^{-3}	E-3
10^{-2}	E-2

B.39 In response to the FR? command, the Transmitter snapshots its current framing mode and queues it for output to the bus. When the Transmitter is in the FRAMED mode, the three-letter ASCII mnemonic FRM is output. When the Transmitter is in the UNFRAMED mode, UNF is output.

B.40 In response to the PA? command, the Transmitter pattern is snapshot and queued for output. Patterns and their corresponding four-character ASCII mnemonics are as follows:

PATTERN	MNEMONIC
pseudorandom bit sequence	PRBS
fixed 1111	1111
fixed 1100	1100
fixed 1010 (blue signal)	1010

B.41 In response to the LV? command, the Transmitter snapshots and queues for output its current transmit level. DSX, LOW, and ␣HI are the ASCII mnemonics associated with DSX cross-connect, LOW, and HIGH level outputs. (␣ is an ASCII space character.)

B.42 Each output mnemonic is followed by an ASCII carriage return and line feed (CR and LF). If the command sequence MD?, RT?, FR? is issued and the Transmitter is currently set up for local control, error-free, 10^{-9} error-rate, framed, the ASCII message queued for output would be LOCFRE CR LF E-9 CR LF FRM CR LF. When the S5200E Transmitter is addressed to talk, queued data are output on the bus. When the Transmitter has no more data queued for output, it will place one or two null bytes on the DIO lines along with the EOI signal.

F. Service Request and Serial Poll Response

B.43 Several conditions detected in the S5200E Transmitter will cause it to request service of the GPIB controller. The ability of the Transmitter to request service may be inhibited by the rear-panel DIP switch as described in Table E.

B.44 When the controller detects a service request, it should serial poll the Transmitter to determine if the Transmitter is requesting service and why. In response to a serial poll addressed to the S5200E Transmitter, the Transmitter will place its 8-bit GPIB status byte on the DI0 lines. The Transmitter clears its status byte when it receives a serial poll disable (SPD) command. The GPIB status byte is also cleared on power-up and in response to device clear (DCL). Only the service request bit in the status byte is reset by an interface clear.

Service Request, GPIB Status Byte

The following Transmitter-Detected conditions will cause it to request service (if SRQ is enabled):

MOST-SIGNIF. HEX DIGIT				LEAST-SIGNIF. HEX DIGIT			
7	6	5	4	3	2	1	BIT ∅
∅	RQS	∅	∅	POWER LOSS	CMD ERR	BUS ERR	TALK REQ

T-160284A

- Bus error — Bus error occurs when the transmitter is addressed to talk with no listeners active on the bus. Since a source handshake may have been started by the

talking receiver with no acceptor to complete the handshake, this error may hang up the bus. This condition can be cleared and detected by the controller issuing an interface clear followed by a serial poll. The ON condition for the bit is 1.

- Cmd error — Command error occurs when the Transmitter detects an invalid device-dependent command as described earlier under Device-Dependent Commands. The command error bit is set in the GPIB status byte. The ON condition for the bit is 1.

- Talk request — When the S5200E Transmitter has data to output, but has not been configured to talk, it will generate a service request with the talk request bit set in the GPIB status byte. The ON condition for the bit is 1. If configured to talk before serial polled, this bit will be cleared in the status byte. If no other bits are set, the service request will be deasserted.

- Inst fail — A software detected failure in the S5200E Transmitter will cause the instrument failure bit to be set in the GPIB status byte. Some instrument failures may not be recoverable by device clear functions. The only recourse, then, is to turn the receiver off and back on. The ON condition for the bit is 1.

- Power Loss — When a power loss is detected, the power loss bit is set in the GPIB status byte. When power is restored, this bit will remain set until either the device clear (DCL) or RESET (RS) command is issued or the Transmitter is serial polled. The ON condition for the bit is 1.

B.45 The RQS bit is ON (1) whenever one or more of the other bits (power loss, instrfail cmd error, bus error, or talk request) is ON and service requests have been enabled by DIP switch 1.

B.46 Multiple bits may be set in the status byte when it is polled. All bits are cleared following a serial poll.

B.47 Status displayed by front-panel LED's is not available through the GPIB status byte acquired by serial polling. The Transmitter status may be obtained as described earlier under S5200E Transmitter Output to GPIB (paragraph B.36).

Serial Polling

B.48 The GPIB status byte may be accessed from the S5200E Transmitter by serial polling as follows:

1. Issue 'UNT' universal untalk command.
2. Issue 'SPE' serial poll enable command.
3. Issue controller listen address.
4. Issue 'MTA' S5200E Transmitter talk address.
5. Receive 'STB' S5200E Transmitter status byte.
6. Issue 'UNT' or 'OTA' S5200E Transmitter untalk command.
7. Issue 'SPD' serial poll disable command.

NOTE: A random loss of the RQS bit may occur after the Transmitter has generated a service request and has been polled. It is recommended that the user check for any bits set in the serial poll status word to determine if the Transmitter may have requested service.

G. Sample GPIB Control

B.49 All S5200E Transmitter functions controllable from the front panel may be remotely controlled using the GPIB. In addition, Transmitter status conveyed locally by front-panel indicators may be accessed under remote control. This section provides samples of GPIB control and status acquisition.

Transmitter Mode Control

B.50 If the user is familiar with the S5200E Transmitter and has operated the instrument manually, then controlling it by GPIB is very simple. Remote control commands exactly imitate front-panel pushbuttons. Consider the following example: Assume the Transmitter is initially set up to generate an error-free, DS3 framed, pseudorandom bit pattern at the DSX signal level. To manually select the same signal level and format at an error insertion rate of 10^{-7}, the user presses the up (arrow) ERROR RATE pushbutton twice to increase the error rate from 10^{-9} to 10^{-7}, then presses the MODE SELECT pushbutton once to change from ERROR FREE to ERROR RATE insertion. Under remote control, the user would simply issue the command sequence UP, UP, MD CR or LF to accomplish the same setup change.

B.51 Device-dependent commands are received by the Transmitter only when it is addressed to listen. The controller must place the Transmitter's listen address on the parallel data lines (DI01-DI08) with the ATN (attention) line asserted to configure the Transmitter to listen. Device-dependent commands are accepted and processed whether the Transmitter is under local or remote control. However, remote commands take effect only when the Transmitter is under remote control.

B.52 When the RE (remote enable) line is asserted and the Transmitter is addressed to listen, its REMOTE CTRL indicator will light and previously issued remote commands will take effect. When the Transmitter is addressed to listen with the ATN not asserted, data placed on the bus is accepted as device-dependent commands (see section E., Device-Dependent Commands). The following example illustrates how the GPIB can be used to select an UNFRAMED PRBS Transmitter HIGH signal with 10^{-4} error insertion rate:

STEP	PROCEDURE
1	With power OFF, set rear-panel DIP switches as follows to enable service requests and select talk address = 41 (hex), listen address = 21 (hex):

SWITCH:	1	2	3	4	5	6	7	8
SETTING:	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON

2	Turn power on.

STEP	PROCEDURE
3	Assert REN line.
4	Issue DCL (device clear) to put Transmitter in known state (error-free, 10^{-9}, framed, PRBS, DSX). Since the Transmitter is still in local control, the new state will not take effect until the Transmitter is addressed to listen with REN asserted.
5	Assert ATN line and issue listen address. Transmitter REMOTE LED will light and Transmitter will go to known state.
6	Issue UP, UP, UP, UP, UP, MD, CR or LF to select 10^{-4} error-rate insertion. This sequence is identical to pushing the up arrow button five times followed by the MODE button.
7	Issue FR, LV, LV CR or LF to select unframed high level signal. This sequence is identical to pushing the FRAME button once, followed by the LEVEL button twice.

Note: Command sequences are output one character at a time and must be terminated by a carriage return and line feed.

Getting Status from the S5200E Transmitter

B.53 After issuing a command sequence such as the one described in the previous example, a controller may wish to verify that the Transmitter has been properly set up. The five query commands (MD?, RT?, FR?, PA?, and LV?) snapshot Transmitter status and queue it for output to the bus. When the Transmitter is addressed to listen, the ASCII-encoded status message will be placed on the DI0 lines. Assuming the Transmitter has been set up as described in the previous example, Transmitter status may be accessed as follows:

STEP	PROCEDURE
1	Assert ATN line and issue Transmitter listen address. Transmitter REMOTE CTRL indicator will remain on.
2	Issue MD?, RT?, FR?, PA?, LV? CR or LF command sequence to query Transmitter mode, error-rate, framing, pattern, and level.
3	Issue universal unlisten command.
4	Configure controller to listen.

STEP	PROCEDURE
5	Assert ATN and issue Transmitter talk address.
6	Receive five status mnemonics from Transmitter, separated by carriage return and line feed. If the Transmitter was set up as described in the previous example, the following ASCII status messages would be returned: REMINS CR LF E-4 CR LF UNF CR LF PRBS CR LF HI CR LF.

APPENDIX C

PERFORMANCE VERIFICATION

APPENDIX C
PERFORMANCE VERIFICATION

A. General

C.01 These tests provide a check of the S5200E Transmitter operation. They also act as an excellent introduction to the operation and capabilities of the Transmitter. The first part of the performance verification tests checks the Transmitter by itself and should be done first. The second part of the tests provides more thorough checks, particularly of the output circuits. This part requires the use of an S5200E Receiver.

B. Transmitter Performance Verification Tests

C.02 These tests of the Transmitter provide checks of the following Transmitter operations:

- Transmitter Power-Up
- Error Mode and Control
- Frame Selection
- Pattern Selection
- Level Selection
- Power Loss Recovery.

Transmitter Power-Up Test

C.03 This test checks the initial power-up state of the Transmitter.

STEP	ACTION	VERIFICATION
1	Press in the POWER pushbutton.	The POWER LOSS indicator lights. This indicates a previous power loss/off state. In addition, one indicator from each selection category and the POWER pushbutton indicator will light.
2	Press and hold the RESET/LED TEST pushbutton.	All the front panel indicators light.
3	Release the RESET/LED TEST.	The POWER LOSS indicator extinguishes pushbutton, and only one ERROR MODE, FRAME, PATTERN, and LEVEL indicator will be lit. If this condition is not obtained, refer to SECTION 7 D General Troubleshooting.

ERROR MODE and Control Test

C.04 This test checks the ERROR MODE pushbuttons and indicators operation.

STEP	ACTION	VERIFICATION
1	Repetitively Press the ERROR MODE SELECT pushbutton.	The ERROR MODE indicators (ERROR FREE, ERROR RATE 10^{-N}, and EXTERNAL ERR INJECT) will light one at a time. When the EXTERNAL ERR INJECT indicator is lit, no number will appear in the single digit LED display. A number between 2 and 9 will appear in the LED display when the ERROR FREE and ERROR RATE 10^{-N} indicators are lit. Also, the LED display brightens when the ERROR RATE 10^{-N} indicator is lit (N is the numeric exponent which appears in the LED display).
2	Repetitively press the ERROR RATE ↓ (down) pushbutton.	The ERROR RATE numeric exponent number (N) in the LED display will increase by 1 each time the ERROR-RATE ↓ pushbutton is pressed until it reaches 9, after which, pressing the ↓ pushbutton does not cause the display to change.
3	Repetitively press the ERROR RATE ↑ (up) pushbutton.	The ERROR RATE 10^{-N} numeric exponent number (N) in the LED display will decrease by 1 each time the ERROR RATE ↑ pushbutton is pressed until it reaches 2, after which, pressing the ↑ pushbutton does not cause the display to change.
4	Set the numeric exponent (N) to 5 and set the ERROR MODE to ERROR FREE.	These settings will be used for the Power Loss Recovery test.

FRAME Selection Test

C.05 This test checks the DS3 OUTPUT FRAME pushbutton and indicator operation.

STEP	ACTION	VERIFICATION
1	Repetitively press the DS3 OUTPUT FRAME pushbutton.	The FRAME indicators, DS3 FRAMED and UNFRAMED, will alternately light.

STEP	ACTION	VERIFICATION
2	Set the FRAME mode to DS3 FRAMED.	This setting will be used for the Power Loss Recovery test.

PATTERN Selection Test

C.06 This test checks the front-panel DS3 OUTPUT PATTERN pushbutton and indicators operation, and the rear-panel SHORT PATTERNS toggle switch operation.

STEP	ACTION	VERIFICATION
1	Set the rear-panel SHORT PATTERNS toggle switch up to the 1111 setting and then repetitively press the DS3 OUTPUT PATTERN pushbutton.	The PATTERN indicators PRBS and 1111 will alternately light.
2	Set the rear-panel SHORT PATTERNS toggle switch to the 1100 position (center) and then repetitively press the PATTERN pushbutton.	The PATTERN indicators PRBS and 1100 will alternately light.
3	Set the rear-panel SHORT PATTERNS toggle switch down to the BLUE (FRAMED); 1010 (UNFRAMED) position and then repetitively press the PATTERN pushbutton.	The PATTERN indicators PRBS and 1010 (BLUE) will alternately light.
4	Leave the rear-panel SHORT PATTERN toggle switch set to the BLUE (FRAMED); 1010 (UNFRAMED) position and the DS3 OUTPUT PATTERN set to PRBS.	This setting will be used for the Power Loss Recovery test.

LEVEL Selection Test

C.07 This test checks the DS3 OUTPUT LEVEL pushbutton and indicator operation.

STEP	ACTION	VERIFICATION
1	Repetitively press the DS3 OUTPUT LEVEL pushbutton.	The LEVEL indicators (HIGH, DSX, and LOW) will light one at a time.
2	Leave the DSX indicator lit.	This setting will be used for the Power Loss Recovery test.

POWER LOSS Recovery Test

C.08 This test checks the Power Loss Recovery function of the Transmitter.

STEP	ACTION	VERIFICATION
1	Press the POWER pushbutton to turn off the power. Press the POWER pushbutton again to power-up the Transmitter.	The following indicators will light, indicating the last control settings have been remembered: • POWER LOSS • ERROR FREE • DS3 FRAMED • PRBS • DSX
2	Press the RESET/LED TEST pushbutton.	The POWER LOSS indicator will extinguish.

C. Transmitter Performance Verification with Receiver Tests

C.09 These tests of the S5200E Transmitter, in conjunction with the S5200E Receiver, should be performed after the tests on the Transmitter alone.

DSX LEVEL, PRBS PATTERN, DS3 FRAME

C.10 Leave the Transmitter set up in the same state as the end of the previous tests on the Transmitter alone, and perform the following setup procedure.

STEP	PROCEDURE
1	Turn the Transmitter POWER ON. Make sure the Transmitter is set as follows:

STEP	PROCEDURE

Front Panel Settings:

- LEVEL = DSX
- PATTERN = PRBS
- FRAME = DS3 FRAMED
- ERROR MODE = ERROR FREE
- ERROR RATE = 10^{-5}

Rear Panel Settings:

- SHORT PATTERNS = BLUE (FRAMED); 1010 (UNFRAMED)

2 Connect the Transmitter to the Receiver using a 75-ohm cable with WECo 358 type plugs.

3 Turn the Receiver POWER ON. The display will read:

"PAR ErrRateNow=0.0E-08, TotalEr= 0"

and the following indicators will light:

- POWER
- UNTIMED
- IN PROCESS
- DS3 FRAMED
- LIVE
- DSX/DSX LOW

4 This setup procedure verifies the Transmitter LEVEL (DSX), PATTERN (PRBS), and FRAME (DS3 FRAMED). If the Receiver is functioning properly and the above conditions are not obtained, there is a problem with the Transmitter. In this case, see Section 7 - SERVICE AND MAINTENANCE.

HIGH/LOW LEVEL, BLUE PATTERN, UNFRAMED

C.11 This test checks the HIGH and LOW levels output by the Transmitter, the BLUE pattern, and the UNFRAMED mode.

STEP	ACTION	VERIFICATION
1	Set the Transmitter DS3 OUTPUT LEVEL to LOW. Set the Receiver DS3 INPUT LEVEL to HIGH/LOW. Press the Receiver START/ RESET pushbutton.	The Receiver display reads: PAR ErrRateNow=0.0E-08, TotalEr= 0
2	Set the Transmitter DS3 OUTPUT LEVEL to HIGH. Press the Receiver START/ RESET pushbutton.	The Receiver display reads: PAR ErrRateNow=0.0E-08, TotalEr= 0
3	Set the Transmitter DS3 OUTPUT PATTERN to 1010 (BLUE).	The Receiver HISTORY and BLUE SIGNAL DETECT indicators light.
4	Set the Transmitter to the UNFRAMED mode.	The BLUE SIGNAL DETECT indicator extinguishes and the FRAME LOSS indicator lights.

ERROR INJECTION

C.12 This test checks that the Transmitter is injecting errors properly.

STEP	ACTION	VERIFICATION
1	Restore the Transmitter front panel settings to: LEVEL = DSX PATTERN = PRBS FRAME = DS3 FRAMED ERROR MODE = ERROR FREE	
2	Set the Transmitter ERROR MODE to ERROR RATE 10^{-5}. Set the Receiver LEVEL to DSX. Press the Receiver START/RESET pushbutton.	The Receiver display will show: PAR ErrRate=1.0E-05, TotalEr= xx

STEP	ACTION	VERIFICATION
3	Set the Transmitter ERROR MODE to ERROR FREE. Press the Receiver START/RESET push-button. Press the Transmitter SINGLE BIT ERROR pushbutton five times.	The display will show: PAR ErrRateNow=0.0E-08,TotalEr= 5
4	Press the Receiver MEAS-UREMENTS CATEGORY pushbutton four times to select the BPV error measurements category. Press the MEASUREMENTS FUNCTION pushbutton. Press the Transmitter SINGLE BPV ERROR push-button five times.	The display will show: BPV ErrRateNow=0.0E-08,TotalEr= 5

BINARY OUTPUTS

C.13 This test checks the binary output of the Transmitter.

STEP	ACTION	VERIFICATION
1	Disconnect the cable from the B3ZS jacks on the Transmitter and Receiver.	
2	Connect BNC cables between the following jacks: Transmitter Receiver BINARY DATA BINARY DATA BINARY CLOCK BINARY CLOCK	
3	Set the Receiver LEVEL to BINARY DATA & CLOCK. Press the Receiver START/ RESET pushbutton.	The Receiver display will show: PAR ErrRateNow=0.0E-08,TotalEr= 0

APPENDIX D
RACK MOUNT OPTION INSTALLATION

APPENDIX D
RACK MOUNT INSTALLATION

D.01 The Rack Mount kit is designed to secure the S5200E Transmitter in a vertical rack. It fits the standard 19-in. (48cm) rack and requires only 8.8 inches (22cm) in height. The depth behind the front panel is 18.5 inches (47cm). For cooling, allow 3 inches (7.5cm) of clearance at the rear and 1 inch (2.5 cm) above and below the unit. Use the following procedure and Fig. 21 to install the S5200E Transmitter into a rack:

STEP	PROCEDURE
1	Remove the AC power cord from the S5200E Transmitter.
2	Remove the existing two front-top and two front-bottom screws from the S5200E.
3	Slide the rack front panel over the front of the unit, and secure with the screws removed in step 2.
4	Reconnect the AC power cord removed in step 1.
5	Mount the rack-mounting bracket to the desired level on the rack, and secure with four rack mounting screws.
6	Install the S5200E, with the rack front panel, into the rack mounting bracket. Secure the front with four front panel mounting screws.

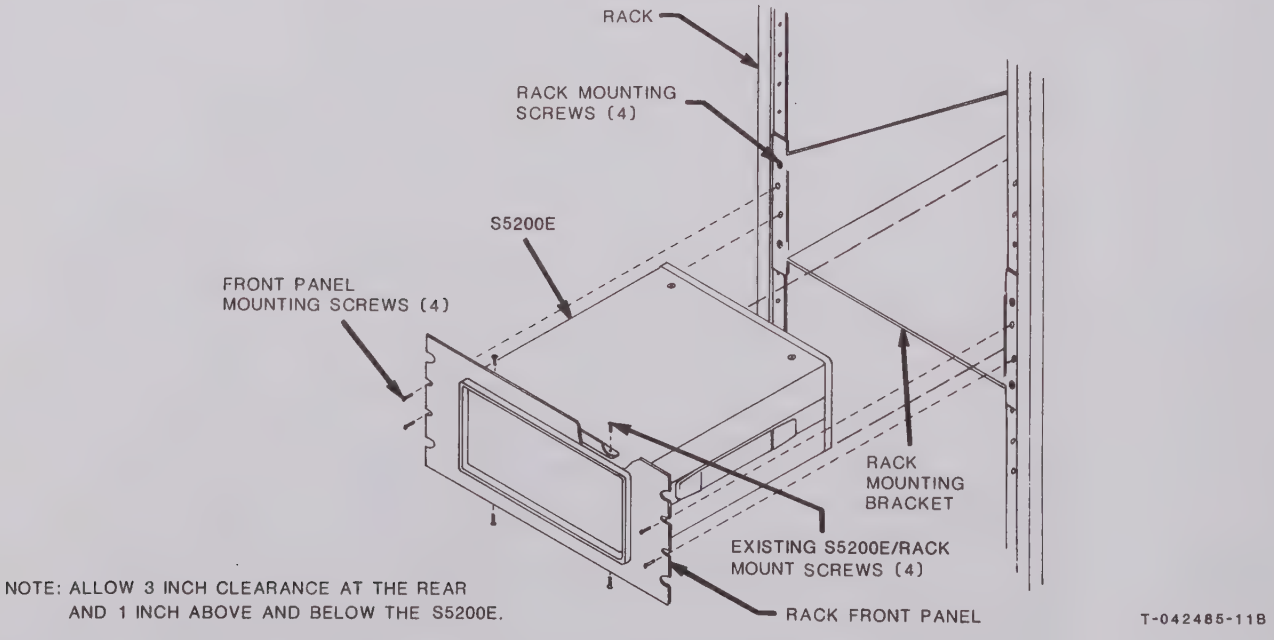

RACK
RACK MOUNTING SCREWS (4)
S5200E
FRONT PANEL MOUNTING SCREWS (4)
RACK MOUNTING BRACKET
EXISTING S5200E/RACK MOUNT SCREWS (4)
RACK FRONT PANEL
NOTE: ALLOW 3 INCH CLEARANCE AT THE REAR AND 1 INCH ABOVE AND BELOW THE S5200E.
T-042485-11B

Fig. 21 - Rackmount Installation

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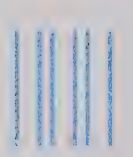

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   Westford, MA 01886
   attn: Customer Service

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Repair Authorization Number _____

Model _____ **Serial Number** _____

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